MIRELAI

MIcroelectornics RELiability driven by Artificial Intelligence
Project no. 101072491

Deliverable 5.3

Computationally efficient submodels

WP 5– Multi-scale modelling techniques

Version 01

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Revision history

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Peter Fuchs (PCCL)	Revision 1	22.05.2024
Julia Zuendel (AT&S)	Revision 2	24.05.2024

Executive summary

Background

The deliverable D5.3 is part of work package WP5 which deals with multi-scale modelling techniques. D5.3 describes computationally efficient submodels and presents the workflow of their implementation in the context of microvias of printed circuit board (PCB) assemblies.

Objectives

One of the objectives within MIRELAI is to generate computationally efficient sub models of defined PCB features. Employing the submodelling technique in simulation allows to accelerate automated parameter studies considering loads and uncertainties under various conditions and also the data generation for the calibration of metamodels.

This deliverable will describe how this approach works and what is its impact on the subsequent research trajectory, with a particular focus on its implications for metamodel development.

Methodology and implementation

In the presented work the submodelling technique is used to evaluate the precise stress and strain characteristics of microvia structures in printed circuit board assemblies. For the method development the global model is a simplified model of a PCB consisting of multiple vias, while the submodel is a detailed model of a microvia with a more refined mesh. Automated finite element analysis (FEA) for a wide range of microvia design parameters are conducted with the aid of Python scripting.

Outcomes

From the FEM simulations, it was demonstrated that microvias with lower wall angles are more vulnerable to failure under thermal loading conditions, consistent with previous literature predictions. Furthermore, the study revealed that variations in microvia radii and angles influence both stress and strain levels, offering deeper insights into the mechanical behaviour of microvias under thermal stress.

One major future approach is the development of a mesh-independent criticality assessment based on a refined mesh, suitable material models and introducing Sub-submodels. This approach aims to maintain computational efficiency, making it suitable for extended parameter studies. The generated data is intended to serve as the basis for training surrogate models, which are expected to enable full-field analysis of all individual vias within a PCBA.

Impact

This deliverable facilitates the calibration of metamodels for applications in criticality assessment. The quality and quantity of data generated from submodels to be used for calibration, directly impact the accuracy and reliability of the metamodel.

Next steps

Next step is to build a metamodel to approximate the relationship between input and the desired outputs based on the submodel data generation. The selection of an appropriate metamodeling technique, coupled with the utilisation of high-fidelity submodel-generated data, together with rigorous calibration and validation procedures, facilitates the development of a robust tool for supporting informed design decision-making processes in the engineering applications.

Contents

Partner short names

Short name	Partner name
PCCL	Polymer Competence Center Leoben
AT&S	AT & S Austria Technologie & Systemtechnik Aktiengesellschaft

Abbreviations

Acronym	Full name
D	Deliverable
EC	European Commission
EU	European Union
FEA	Finite Element Analysis
HEU	Horizon Europe
M	Month
MS	Milestone
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
WP	Work Package

1 Introduction

There is continuous demand in the electronics industry for smaller, lighter, and more efficient electronic devices, which has led to the development of advanced technologies like microvia technologies. These technologies are integral to achieving high-density interconnections in printed circuit boards (PCBs), catering to the demands of modern electronics such as portable computers and wireless communications.

Submodelling, a technique employed in finite element analysis (FEA), has emerged as a powerful tool in the field of microelectronics for analysing and optimising the behaviour of microscale components. As microelectronic devices continue to shrink in size and diverge in complexity, traditional modeling approaches often struggle to accurately capture the intricate interactions and localised phenomena occurring within these devices. Submodelling offers a solution by allowing for the refinement of the computational mesh and the application of more detailed geometries within specific regions of interest, enabling a more accurate representation of localized effects.

The basic workflow is to build a coarse model, also known as global model to represent the complete microelectronic device. Then the critical region, e.g. a local region encompassing a microvia, of the structure is identified. The characteristics of the local region is then re-evaluated after employing submodel with a more refined mesh. The forces and displacements at the boundary of the local region and the rest of the microelectronic device will define the interaction of the submodel with the rest of the global model [1].

Submodelling finds widespread applications across various domains within microelectronics. It facilitates the detailed analysis of stress, strain, and deformation within critical components such as microvias, solder joints, and interconnects. By refining the mesh and applying advanced material models, submodelling enables engineers to accurately predict failure modes and improve the reliability of microelectronic devices.

Submodelling facilitates the simulations of complex microelectronic structures much faster and efficient. Submodelling allows for the optimization of microelectronic designs by focusing computational resources on specific regions of interest. Engineers can iteratively refine the design based on submodel analysis results, leading to improved performance, efficiency, and manufacturability [2, 3].

In thermal management applications, submodelling enables the precise prediction of temperature distributions and thermal gradients within microelectronic devices. This information is crucial for optimising heat dissipation strategies and preventing thermal-induced failures.

It is to note that submodelling can also facilitate the characterisation of material properties at the microscale, including mechanical, thermal, and electrical properties. By applying submodels to localised material specimens, researchers can obtain accurate material behaviour data for use in macroscopic simulations.

1.1 Current challenges

Despite its numerous benefits, submodelling in microelectronics also faces several challenges. Primarily, submodelling results may be sensitive to changes in mesh density and element types, requiring careful mesh refinement and validation to ensure accurate results. Validating submodels against experimental data remains a challenge, particularly for complex microelectronic systems with multiple interacting components. Further, the submodelling can be computationally expensive, especially for large-scale microelectronic systems with numerous submodels, necessitating efficient computational strategies and algorithms. In addition, the integration of submodelling techniques into existing design tools and workflows requires a major effort to achieve seamless interoperability and compatibility.

1.2 Possible solutions

To address these challenges and advance the state of the art in submodelling in microelectronics, future research directions may include:

- Continued development of material models tailored specifically for microelectronic applications, accounting for nonlinearities, anisotropy, and other complex phenomena.

- Integration of machine learning algorithms for automated mesh generation, adaptive refinement, and model calibration, improving efficiency and accuracy.
- Development of standardised validation frameworks and benchmarks for submodelling techniques in microelectronics, enabling more rigorous validation and comparison of results.
- Advancement of multi-physics simulation techniques that integrate mechanical and thermal analyses within a unified framework, capturing the full complexity of microelectronic systems.

2 Methodology

The methodology employed in the study utilises submodelling techniques within the framework of FEA to assess the criticality of microvias in printed circuit board assemblies (PCBAs). This methodology section outlines the steps taken to model and simulate the thermomechanical behaviour of microvias, focusing on the analysis of geometrical design parameters (Figure 1) of microvia, layer thickness of prepreg and copper (Tables 1 and 2), and finally their impact on reliability.

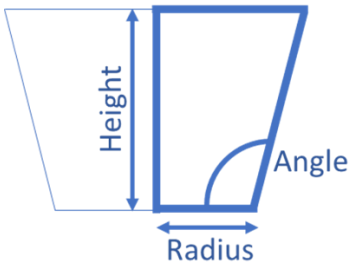

Figure 1 Schematic representation of the analysed microvia design parameters [3].

Table 1 Dimensions of copper and prepreg layers (based on [3]).

Material	Dimensions (L x W x H) (µm)
Copper layer	600 x 600 x 15
Dielectric layer (prepreg)	600 x 600 x 65

Table 2 Different microvia parameters considered for the studies (based on [3]).

Parameters	Variations
Microvia angle (°)	90, 100, 110, 120, 130, 140, 150
Radius (µm)	40, 45, 50, 55, 60, 65, 70, 75, 80
Height (µm)	65

The implementation begins with the creation of both global and local FEA models using commercial software. The global model represents a highly simplified PCB layout featuring multiple microvias, while the local model isolates a single microvia from the global configuration (Figure 2). This approach allows for a detailed

examination of the stress distribution within individual microvias while considering the influence of the overall PCB design.

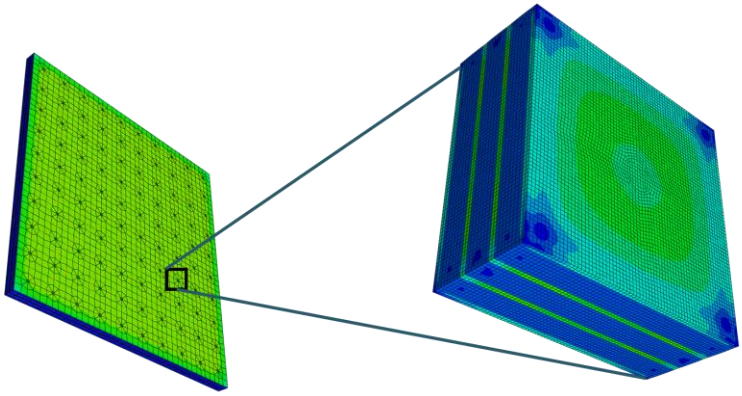

Figure 2 Depiction of Global model and submodel (The global model mesh size was 0.5 mm compared to the submodel mesh size of 0.009 mm).

The loading conditions for both the global and local models are defined to simulate the thermal loading experienced during the PCB assembly process, ranging from 20°C to 260°C to mimic the reflow process. The models are meshed, with a finer mesh employed in the local model to capture localized effects accurately. The element type employed was hexahedral, namely the C3D8R, which are 8-node linear brick elements with reduced integration and hourglass control.

Material properties and calibrated material models are applied to both the copper and dielectric layers based on prior research and experimental data. In the presented study a linear elastic temperature dependent material model was applied for prepreg and copper. Future work is planned to incorporate advanced material models considering damage accumulation.

Python scripting is employed to automate the generation of FEA models for various combinations of microvia design parameters, including microvia angle and radius. This allows for the efficient exploration of a wide range of design scenarios and facilitates the analysis of stress and strain distributions [4, 5].

In summary, the methodology employs submodelling techniques to comprehensively assess the criticality of microvias in PCBAs, providing valuable insights for optimising microvia design and enhancing reliability in electronic packaging applications which can be seen in detail at our publication [3].

3 Results

The outcomes of the study reveal several key findings regarding the criticality assessment of microvias in PCBAs. To assess the influence of different geometric via design parameters the maximum Mises stress was evaluated for each configuration at the upper edge between pad and via. The stress results for all elements around the via in this region have been averaged and have been considered for the comparison (see Figure 3). The authors are aware of the mesh size effect at sharp edges but considered the results for a trend analysis only. Firstly, the analysis underscores the vulnerability of microvias with lower wall angles to failure under thermal loading conditions. Lower wall angles have been identified to increase the stress concentration at the critical edges. Lower microvia radii again lead to reduced maximum stress due the reduced via stiffness and lower out-of-plane thermal expansion mismatch with the dielectric material (compare figure 4). The results have been found to be consistent with previous literature predictions [6].

These findings emphasise the importance of meticulous microvia design considerations in mitigating vulnerabilities and enhancing reliability in electronic packaging applications. Furthermore, while the study acknowledges certain limitations such as mesh size effects and the use of simplified material models, it lays

the groundwork for future research aimed at developing more advanced analysis techniques to improve accuracy and reliability assessments.

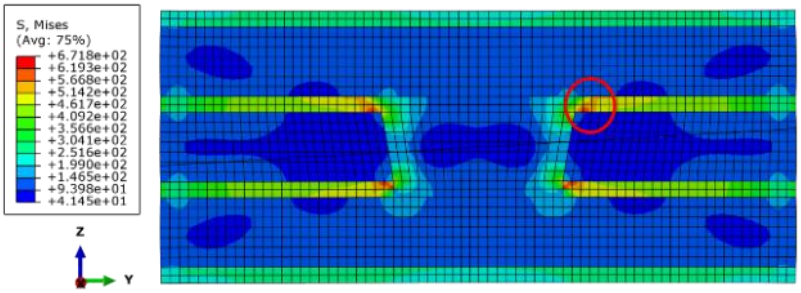

Figure 3: Cross-section of a microvia submodel with 80um radius and 100° angle. The red marking shows the stress peak and indicates the evaluation region [3].

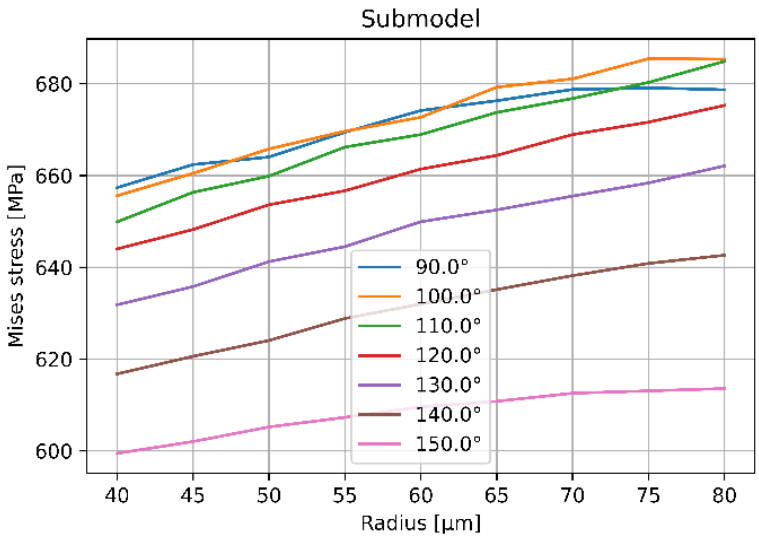

Figure 3 Mises stress distribution in submodel over microvia radius at different microvia angles [3].

A simplified material behaviour has been assumed and no anisotropy, viscoelasticity, plasticity or damage parameter was considered for the time being, as the initial focus of the presented work was on the method development only. Future work will be concentrated on adapting plasticity of the materials, anisotropic constraints and suitable viscoelastic parameters.

Individual combinations of the microvia diameter and microvia angle simulation takes around four to five hours but by using automated script for all diameter and angle combinations (63) takes around 19 hours in total.

4 Future work

While WP5 demonstrates the effectiveness of multi-scale modelling for criticality assessment, future work will focus on developing computationally efficient submodels to further reduce the time and expertise required for this process.

Metamodel Development:

- We will explore the creation of metamodels trained on the simulation data generated from WP4's package and PCB-level models (detailed in deliverables D4.1, D4.3, and D4.4).
- These metamodels will capture the essential relationships between design parameters and submodel behaviour, enabling rapid and consistent predictions compared to traditional multi-scale modelling approaches.

Automating Sub model Generation:

- We will investigate the possibility of automating submodel generation by leveraging machine learning techniques. This would involve training algorithms to identify critical features and automatically construct corresponding submodels, reducing the need for extensive manual expertise.

Uncertainty Quantification:

- We will extend the metamodels to incorporate uncertainty quantification, allowing for the propagation of material and design uncertainties through the system-level model. This will provide more robust reliability predictions while considering inherent variability in real-world components.

By focusing on these future directions, WP5 aims to significantly reduce the computational cost and expertise required for multi-scale modelling in future projects, making it a more accessible and practical tool for reliability assessment in electronic systems.

5 References

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