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Deliverable 4.3

Definition of critical weak links and PoF literature review

WP4 – Physics of degradation

Version 1

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Revision history

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Executive summary

Background

The deliverable D4.3 is part of work package 4 (WP4). In WP4 Physics of degradation, test methods will be developed to gain an understanding of the physics of relevant failure mechanisms and to identify material and process uncertainties.

The specific aims are as follows:

1. Identification of uncertainties of all analysed materials and processes applied within the research projects and summary of the findings in a common database.
2. Description of the degradation development behaviour as input for the physics-informed learning (function or interrelation).

Deliverable D4.3 presents the definition of critical weak links and physics-of-failure approaches. The deliverable is based on literature review in DC’s 1, 4, 6, 10, 12 and 13.

Objectives

One of the objectives within Mirelai is to identify critical weak links in semiconductors devices using physics-of-failure approaches. This deliverable will describe how these approaches evolved over the years and what the current state-of-the-art is.

Methodology and implementation

Extensive literature review is done by DC’s 1, 4, 6, 10, 12 and 13 to scope the field of physics-of-failure. Implementation is done by distributing this deliverable to all other DC’s.

Outcomes

Regarding physics of degradation, the DC’s 1, 4, 6, 10, 12 and 13 literature review demonstrate the limited number of publications in this area. Physics of failure is well described but the actual degradation processes are not well known.

Impact

This deliverable will set the pace on the physics of degradation subject that is central within the Mirelai project. For each DC within the project this deliverable will provide an excellent benchmark information regarding physics of failure research done in the past 10 years.

Next steps

With the literature review done for DC’s 1, 4, 6, 10, 12 and 13, the next step is to define the academic parts of their research: what areas are new and can be further explored?

Contents

Partner short names

Short name	Partner name
PCCL	Polymer Competence Center Leoben
POLIMI	Politecnico di Milano
TU Chemnitz	Technische Universität Chemnitz
TU Delft	Technische Universiteit Delft
IMEC	Interuniversitair Micro-Electronica Centrum
ams OSRAM	Ams-Osram AG
AT&S	AT & S Austria Technologie & Systemtechnik Aktiengesellschaft
Bosch	Robert Bosch GmbH
Nanotest	Berliner Nanotest und Design GmbH
Nexperia	Nexperia BV
NXP	NXP Semiconductors Netherlands BV
SISW	Siemens Industry Software NV
Technoprobe	Technoprobe SPA
UOG	University of Greenwich
MCS	Materials Consultancy Services Limited
accelCH	accelopment Schweiz AG
KU Leuven	Katholieke Universiteit Leuven
MUL	Montanuniversität Leoben
MCL	Materials Center Leoben Forschungs GmbH
signify	Signify Netherlands BV

Abbreviations

Short name	Partner name
D	Deliverable
EC	European Commission
EU	European Union
HEU	Horizon Europe
M	Month
MS	Milestone
WP	Work Package

1 Introduction

The history of reliability as we know it now goes back to the 1950s, when electronics started to play a major role for the first time. Now, 7 decades later, with million times more complex electronic systems, the industry is facing a continuous increase of early and wear-out failures with accompanying consequences. Nowadays, products with high failure rates may come under public scrutiny due to negative customer feedback publicly shared on websites, eventually building bad reputation for a company [2]. To cover the increasing demands in product reliability performance, three distinct waves can be noted [3]:

- Wave 1: Stress based

The first wave was characterized with the establishment of a test-to-failure approach based on standardized stress-based tests. Examples are thermal cycling, moisture testing and/or operational tests under combined conditions. Each of these tests got standardized in the semiconductors industry by dedicated bodies, like e.g. JEDEC, IEEE or IEC [4, 5], to enable smooth comparison between suppliers and test houses. Understanding of possible failure modes gradually increased in several industries using semiconductor devices but the use of prediction models was still limited.

- Wave 2: Knowledge based

The second wave continued from all the test results obtained over a period of 30-40 years in the first wave. Companies started to understand the physics that caused failure modes in their products. Test schemes changed to test-to-failure instead of test-to-pass. Still standardized tests are used under the condition of similarity: if a previous product that differed slightly from a new one, no new testing was required. This wave is characterized as knowledge-based qualification [6]. Models became commonly used in this wave both analytical and / or numerical (using Finite Element methods) ones.

- Wave 3: Application based

In the third wave, application conditions are considered. All industries performed a substantial amount of application studies in which dedicated sensors are used to measure the actual loading, in terms of temperatures, vibrations and/or external forces. Here measure, in some cases, means monitoring so that the data is logged continuously and sent to an on-line database. Although standards are not yet available, some bodies did publish guidelines [7].

Nowadays, most industries are in the transfer coming from wave 2 towards wave 3. Wave 3 goes hand in hand with the current development of machine learning, digital twin driven diagnostics or prognostics and health monitoring [8]. These technologies are needed to move to *Wave 4: Physics of Degradation and Robustness.* These two new concepts will become available at a significant level of maturity.

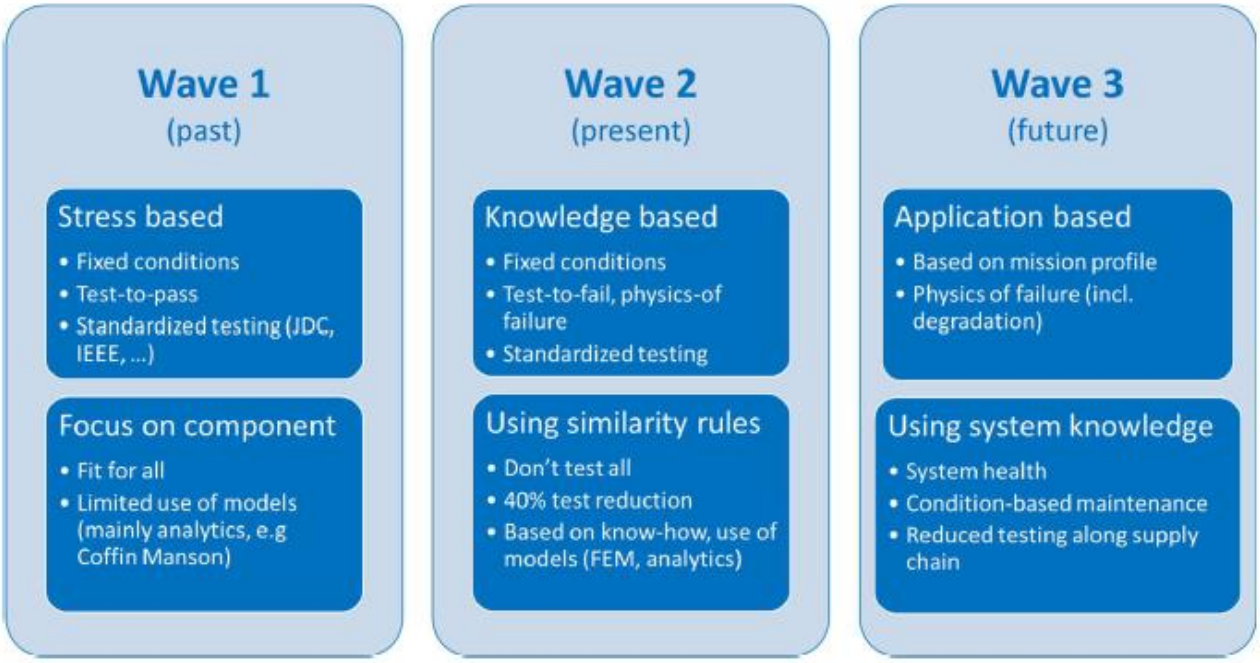

Figure 1 Waves in reliability.

1.1 Physics of Degradation

Degradation is apparent in all things and is fundamental to both manufactured and natural objects. It is often described by the second law of thermodynamics, where entropy, a measure of disorder, tends to increase with time in a closed system. Simply said things age. The natural ageing and degradation of materials has been a subject of study by engineers and scientists for many, many years. But with the demands placed on new engineered materials and devices for electronics, computing, aerospace and biomedical applications, the reliability of such over time has become more and more crucial [9, 10].

Degradation is apparent in naturally occurring materials and structures as well as human-engineered materials and devices. In everyday experience, it is the ever-present phenomena of spontaneous loss of some quality, functionality, and order. Work must be done from outside the system of interest to maintain that functionality, or that order. The second law of thermodynamics formally captures this idea with the concept of entropy or disorder, which states [10]:

> *During real processes, the entropy of an isolated system always increases. In the state of equilibrium, the entropy attains its maximum value.*

This loss of order or degradation has many terms or phrases to label the phenomena, such as ageing, deterioration, devolution, and wear-out.

The mechanisms of degradation for a variety of materials and structures cover a wide range of discipline categories such as thermal, mechanical, chemical, biological, and so on. All associated degradation mechanisms require the knowledge and understanding of natural processes and thus are grouped together as the physics of degradation. As mentioned above, the fundamental underlying principle is entropy and the second law of thermodynamics. Health monitoring [8] and/or digital twin technologies [11, 12] may support the engineers to understand, master and forecast the physics of degradation. The concept of digital twin is relatively new. It was conceptualized during the early years of the 21st century and has gained traction mainly during the last decade. The primary reason behind it is the further digitalization of the electronic industry, which has been accelerated by the newly emerging IT technologies. Here, digital twin can be defined as [13]:

> *Digital Twin is a continuously updated multi-physics, multiscale, probabilistic simulation model of a physical entity (an object, a system, or a process) utilizing big data, bilateral connectivity, and advanced software analytics to provide product monitoring, diagnostics, prognostics, and optimization services.*

Digital twin enables system optimization, monitoring, diagnostics, and prognostics using integration of artificial intelligence, machine learning, and big data analytics. It can be used for predicting failures and estimating lifetime of electronic components, which then allows for scheduling preventive maintenance. Launching a preventive maintenance program like this allows company to save time and costs and avoid customer dissatisfaction as well as unwanted lawsuits.

1.2 Robustness Validation

Today's standard qualification procedures for electronic components, assemblies and components for the automotive industry are based on the use of standardized tests at the end of the product development of parts and components. In contrast, Robustness Validation is a process that includes the entire product development process, as well as mass production. The qualification of the components based on the robustness analysis is thus implicit. The basic philosophy behind the robustness validation methodology is to gain knowledge about the size of the guard band by testing the semi-conductor to failure, or end-of-life [14, 15]. The goal of the method is to achieve lower ppm-failure rates by ensuring adequate guard band between the ‘real-life’ operating range of the semiconductor and the points at which the semiconductor fails. The concept of robustness validation is relatively new and during the early years of the 21st century gained traction mainly during the last 5-10 years. It found its origin in the automotive industry [16]. The new 'test to fail' qualification approach (instead of a 'test-to-pass'), is a paradigm shift from 'Fit for Standard' to 'Fit for Application'. Therefore, components could be designed with known robustness margins combined with cost and time saving potentials. The principle of robust validation is depicted in Figure 2.

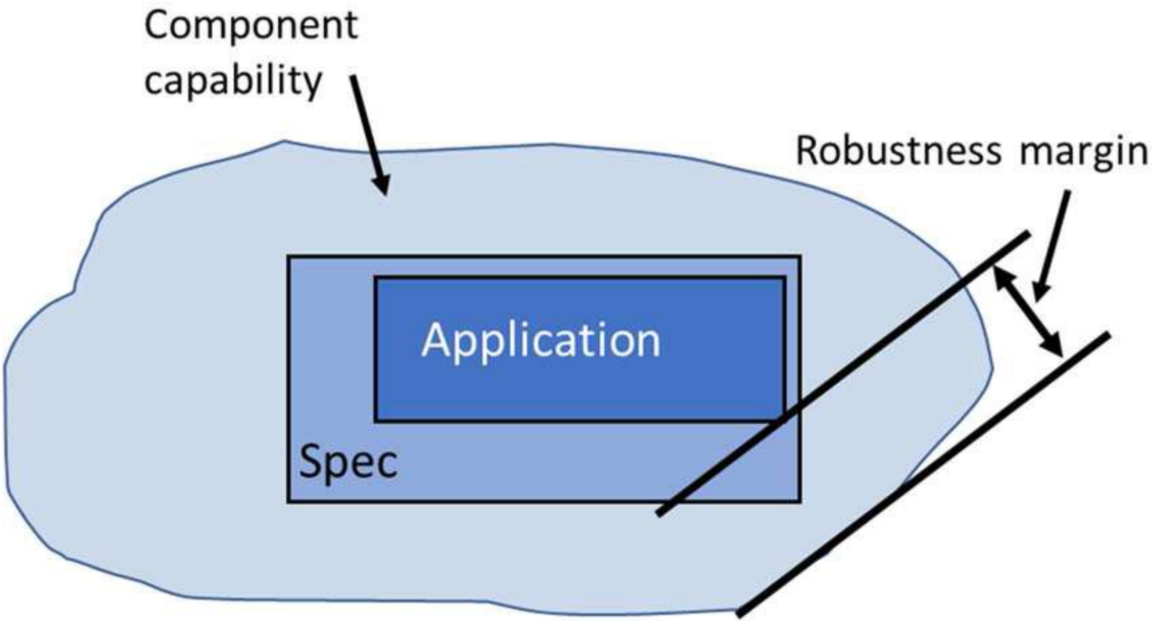

Figure 2 Schematic illustration of the basic idea of robustness validation

2 DC literature review

In the next paragraphs, the DC's involved in this subject will present their literature review. It is organized as such:

- DC1: Criticality assessment methodology for PCBA features by Vikram Kamble
- DC4: Accurate digital twins on component level by Alireza Mehrabi
- DC6: Reliability of IC packages under small loading conditions by Mohammad Musadiq
- DC10: Microstructure Informed Modelling and AI for Reliability Predictions by Najeem Muhammad Umair
- DC12: AI-assisted design of high-performance and high-reliability probe technologies for EWS applications by Imtiaz Shehryar
- DC13: AI-assisted study and forecast of field performances of probe cards for EWS applications by Bejani Mehidi

For easy of simplicity, each chapter uses its own reference list.

2.1 DC1 Criticality assessment methodology for PCBA features

2.1.1 Introduction

Three-dimensional (3D) semiconductor integration could help electron devices overcome Moore's law. Using the third-dimension increases density, functionality, and performance per unit area. The widespread deployment of 3D integrated technology confronts various obstacles before mass production is possible. Direct silicon connections integrate 3D components most directly and efficiently. These connections involve silicon substrate-crossing through-silicon vias (TSVs) and microvias. These vias typically have sizes between 50 μm and 300 μm [1,2].

SiO2 has the lowest CTE, hence copper plugs' lateral expansion increases SiO2 liners' tensile stresses. This can shatter silicon substrates or SiO2 insulators. Even if stresses do not induce die failure, they can impair transistor mobility and parametric shifts, reducing IC performance and via tolerances 10. Silicon's carrier mobility changes by 7% at 100 MPa 11 and saturation current by 2% to 4% at 200 MPa 12. Although these effects can be minimized, Bosch deep reactive ion etching (DRIE) [3] via sidewall scallops increases stress concentration in SiO2 liners and barriers, increasing the risk of reliability issues like insulator failure, current leakage, copper diffusion, and electromigration [4].

Copper pumping reliability issues arise from vertical copper plug expansion. Pumping can delaminate copper plugs at the liner interface, collapse micro bumps, and damage inter-dielectric layers [5]. Copper plugs release all volume expansion during vertical growth because substrates have a lower CTE, limiting lateral thermal expansion. Thus, Cu pumping and dependability issues increase. These concerns can be addressed with stress buffer layers with polymer insulators, open topologies, or polymer cores in annular conductors. These methods reduce heat stress. Polymers lessen heat stresses due to their low elastic modulus and deformability [6].

For the microvias and its surroundings, researchers built finite element (FE) numerical models to determine locally generated stress and strain values. Analytical models predicted microvia fatigue life. Ogunjimi et al. [7] found that strain concentration factor, copper ductility, and microvia wall thickness affected microvia reliability more than wall angle and epoxy height. Ramakrishna [8] and others utilized FEA to explore how geometry and material parameters affected microvia dependability and found that wall thicknesses, angles, diameters, dielectric thicknesses, and quality affect stress and strain levels. Wang and Lai [9] evaluated MCM substrate microvia failure areas using FEA submodelling. They found that complete microvias are less stressed in their model. The literature examined single-level flaw-free microvias using FEA. Pecht et al. studied voiding and incomplete microvia filling [10].

2.1.2 Microvia failure

Misregistration, barrel cracks, corner fractures, target pad cracks, interface separations, and stacked microvia failure mechanisms are microvia failure modes. Categories are based on impact and damage buildup mechanisms of failure. The microvia-to-target pad contact and microvia cross-sections are examined for failure. Internal copper layers, plated thicknesses, and crystalline structures are revealed via micro-etching. Controlling micro-etching increases physical details and helps identify failure causes.

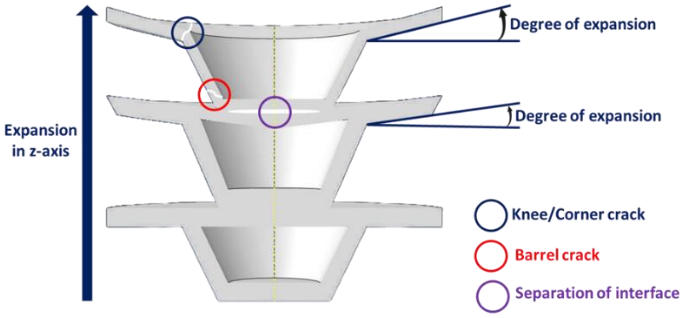

Figure 3: Depiction of thermal expansion in microvia system and related cracks.

Interface separations

A gap between the microvia's base and pad causes most failures (Figure 3). This mechanism often fails during cooling. This condition has many causes, including:

- Insufficient resin removal during ablation creates a nonconductive barrier between metallization and target pad.
- Insufficient micro-etching on the target pad hinders chemical bonding. Chemical interaction is weakened by ash deposit between metal layers.
- Lack of electrolytic copper on target pad hinders good connection.

Microvia barrel breaks

Thin electrolytic copper plating connects barrel cracks, which taper towards the microvia's base (Figure 3). They usually result from plating-process chemistry and mechanical imbalance.

Printed wire board (PWB) manufacturers may utilise different chemical vendors for metallization, which might produce chemical incompatibilities between crucial phases. The chemical and equipment suppliers should collaborate to make reliable microvia structures. Capability and compatibility depend on equipment type. Reliability testing indicates microvia barrel cracks wear out. Although the via may withstand assembly stress without breaking, the conductive channel will degrade and open.

Microvia knee/corner cracks

When extensive copper removal (planarization) leaves just thin pads, the pad-via plating interface might become unstable, causing microvia knee or corner cracks. Figure 3 shows how this can harm during thermal expansion.

Pad rotation damages a “butt-joint” interface between the pad and through plating when knee/corner plating is removed. Excessive z-axis dielectric expansion between the capture pad and target pad during component assembly or local rework damages the pad. CTE is unlikely to damage or propagate a crack at the normal operating temperature and dielectric distance between the layers, which is usually 0.05 mm (.002 in) to 0.15 mm (.006 in). Mechanical stress “pulling” the pad off the upper microvia segment would increase pad rotation due to the PWB-device CTE mismatch, generating this failure scenario. The surface pad is almost peeled off the resin, like pad cratering. Damage to the microvia-surface pad junction could cause this failure condition. Microvia knee/corner cracks fade after beginning.

Microvia misregistration

Failures might come from microvia misregistration. Short circuits can result from improper hole ablation or layer alignment. Manufacturing tolerances cause statistically inevitable misalignment in stacked microvia structures.

Ablated capture pad or target pad holes can misregister single-level microvia. Automatic test equipment from PWB manufacturers can detect holes or shorts in both cases. Laser ablation of dielectric material at the pad edge may penetrate an underlying feature, creating z-direction short circuits. Due to its narrower dielectric gap, it is susceptible failure. A microvia misregistration may not reduce heat cycles to failure unless the lower contact area compromises target pad adhesion. Stacking microvia architectures have registration challenges since each lamination cycle must account for manufacturing tolerances.

2.1.3 Microvia assessment and their failure techniques

Current microvia inspection demands quick and cost-effective characterization of hundreds or thousands of them, together with statistical data, location and condition information, and via failure categorization. Such faults are often found using nonautomated laboratory methods like SEM, XCT, EMMI, and SAM. They also use automated methods like EM, AOM, and SAM. Each strategy has pros and cons that restrict its utility. EM can quickly and widely detect vias breakdown but cannot localize it. Bottom defects are detected well by AOM, while sidewall faults are not. SEM provides high-definition sidewall and via bottom images but is too slow for high-throughput inspection. Limitations of SEM and XCT include scanning duration and resolution. SAM can swiftly characterize broad areas nondestructively, but its resolution and contrast are limited and require post-processing to retrieve relevant information [11,12].

Microvias stress analysis

The researchers examined how thermal processing stresses open microvias' metal layers. They model low-temperature plastic deformation and dislocation glide. Tungsten layer model parameters were determined and validated. Comparing simulated and experimental data shows the method's accuracy. The geometrical effect on temperature change affects via stress. Thermal dips between scallops in microvias are crucial for structure mechanical durability [13–15].

The inherent and thermal stress components are separated using FE models and observed stress through a flat tungsten film. Findings [16] evaluated tungsten metal layer tension in an open microvia structure with scalloped sides. Simulation results match synchrotron X-ray nano diffraction results. Parallel simulations examined how flat and scalloped microvias varied in electrical performance and stress. The researchers found that scallops increase resistance, inductance, and parasitic capacitance. The current path through bent and extended tungsten metal 99 increases resistance and inductance. However, scallops increase capacitance due to electric field peaks in the separated oxide material. Concave pieces become convex when deposited on an etched silicon trench, and vice versa. Thus, the scallop pinch-off areas have a lower oxide effective thickness, increasing the electric field and coupling capacitance. The scallops slightly lessen the average tungsten layer stress, although it still has peaks and valleys along microvia sidewall [17].

Thermomechanical dependability of microvias

The researchers [17] studied how sidewall scallops affect microvias' thermomechanical dependability, considering self-heating and residual stress. Current density, temperature, heat flow, and stress on vias were studied using multi-physics field simulation and submodelling. Sidewall scallops from Bosch etching can cause periodic fluctuations in current density, heat flux, and stress, increasing interfacial failure risk. Polyimide through liners can reduce scallop-induced fluctuations and improve via electric-thermomechanical reliability in via-last integration schemes. The via-last method for depositing SiO2 liners cannot completely remove scallops, which can cause current density, heat flow, and stress variations and interfacial failure.

This study investigated a method for numerically evaluating freshly designed PCBs in interconnection stress tests (ISTs) [18]. The method is based on thermal cycling of a PCB, where the stress-strain response causes a distribution of pore volume fractions that degrades current route conductance. The results of simulated pore fraction evolution-related resistance increases were compared to test data. A well-calibrated pore fraction evolution law may forecast the electrical performance of various PCB designs and reveal their initial pore volume fraction. This method improves evaluation [19].

The researchers examined how voids affect copper-filled stacked microvias' thermomechanical reliability under thermal cycling. Parametric study [19] found that void forms, sizes, locations, microvia aspect ratios, and dielectric material parameters affect cycles to failure. The findings enable OEMs and board makers build HDI board acceptability requirements for cross-sectional and X-ray inspections. Due to localized stress concentration, large spherical voids may degrade thermomechanical reliability, whereas small ones may have a longer fatigue life due to compliance and strain redistribution. The size of the transition vacuum determines its fatigue life.

The CTE mismatch between microvia metallization and dielectric materials fatigues substrates and PCBs. FEA studies have examined strain/stress distribution in parts via filling and voiding. While small voids may increase stress levels, fully copper-filled microvias had lower stress levels than partially filled ones. A little void reduces thermomechanical stress, while copper filling reduces stress overall. FEA simulations show how partial copper filling and plating voids impair microvia reliability [20].

Deep learning-based microvia failure detection and prevention methods

Modern non-destructive failure analytics rely significantly on AI and ML. These industries include aerospace, rail-track inspection, civil engineering, automotive, power generation, and microelectronics. Previously reliant on human experience, ML methods enable complex dataset failure analysis. Many ML models have been utilized to study 3D integration components, which are valuable in microelectronics [21].

These methods fail for generalized analysis since training feature definition is required. Supervised semi-automated ML methods like KNN and Random Forest classifier [22] identify gaps in 3D IC component vias. Wang et al. [22] demonstrate that training such models requires specialized feature extraction. This includes the High-Frequency Structural Simulator (HFSS) data for the "vias with" and "vias without" void. Bradley and Roth [23] use a semi-automated method to find via functional issues like open and short circuits.

The researchers [24] built a convolutional neural network (CNN)-based approach to characterize thousands of vias on the wafer level, find defective vias, classify vias by defect severity, and collect statistical data about the classed vias. They produce picture data for industrially important via arrays with thousands of vias using a unique SAM approach. As shown with AOM, SAM can collect data from the through sidewall and bottom with increased detection sensitivity. Fully automated "E2E-CNN" workflow provides 100% localization and over 96% classification accuracy, respectively.

The fact that pattern recognition algorithms depend on visual input quality is a major limitation. Identifying the through requires adequate image resolution and contrast. Pixel brightness modifications (such as histogram equalization) or thresholding methods like adaptive thresholding [23] or binary thresholding [25] may improve SAM C-SCAN image quality for later processing.

Researchers [26] suggested ANNs for runtime reliability management stress estimation. The unique method generates an ANN-based stress model by offline training with temperature and stress data. For runtime reliability management, the ANN stress model estimates maximum stress around each route. The researchers tested three ANN types: standard, hand-crafted feature extraction, and CNN. This is because the ANN stress model can use numerous ANN architectures.

The new runtime stress estimate method is tested with three ANN stress models with different layer configurations. In real time, reliability increase allows the novel approach to estimate key stress data quickly and accurately [27]. To process, manufacture, and perform with microelectronic devices, 3D integration technologies must overcome many challenges. Recent advanced reliability research [26] focus on via failure analysis and fault discovery, which are difficult.

Because voids and connection failure during manufacture influence vias [28] reliability, extended testing and human judgement are required. Due to the increased demand for vias in 3D IC, reliability analysis and failure prediction have gained focus. The study uses CNN-based machine learning and 3D X-ray tomographic images to evaluate interconnects non-destructively. Training with a reliable library of non-destructive 3D X-ray tomographic images [26] allows the AI to quickly identify and predict interconnect operational problems with 89.9% accuracy.

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2.2 DC4 Towards a Digital Twin Concept for Power Electronics

The fundamental concept of creating a Digital Twin to study a physical object goes back to the 1960s when NASA developed the first digital twin model for testing rescue missions of Apollo 13 in space. In the literature, numerous definitions of the digital twin exist. One of the most intriguing definitions was put forth by NASA's scientists in 2012 in the field of aerospace engineering: "A Digital Twin is an integrated multiphysics, multiscale, probabilistic simulation of an as-built vehicle or system that utilizes the best available physical models, sensor updates, fleet history, etc., to mirror the life of its corresponding flying twin"[1]. Initially, a digital twin model was defined as a three-dimensional model consisting of a physical space, a virtual space, and the connections between them [2]. However, Tao et al [3] proposed a five-dimensional digital twin, which includes a physical space, a virtual space, an updating engine, a predicting engine, and an optimization engine. With continuous development in the field of digital twins, the application of digital twins has expanded to cover more areas every day; for instance, it now includes aerospace engineering, workshop production, electronic engineering, ship automobiles, construction, logistics, and other fields [4].

In the field of the electronic industry, the utilization of digital twins is recommended for the reliability analysis of various devices. For example, Adam Talen et al[5] created a 5D digital twin model of a Li-ion battery to predict its ideal retirement time. Similarly, in [6], it is proposed as a potent tool for diagnosing and prognosticating the health of light-emitting diodes, serving as the connection between the physical space and the virtual space to enhance the accuracy of health monitoring systems.

2.2.1 Semiconductor power devices

Today, most automation and control systems require more flexible energy conversion systems to control voltage, current, frequency, phase changes, and other parameters. In this context, power electronic devices represent the most advanced technology for conserving electrical energy with high flexibility and efficiency. The control of this conversion is integrated into power electronics converter devices, which consist of active components (such as semiconductors), passive components (like capacitors, transformers, inductors), and a control unit (including signal converters, DSPs, sensors, etc.). When designing a power converter, an essential aspect to consider is thermal considerations, including device losses, cooling, and the maximum operating temperature, which determine the physical limits of the converter design. When devices operate within their electrical safe operation area (SOA), conduction and switching losses become the dominant factors contributing to device losses. Moreover, to select the power semiconductor as the core of power converter devices, factors like its switching power and maximum switching frequency are crucial. Currently, several device structures have been developed, each offering specific advantages. Figure 4 illustrates the practical application range of each type of silicon device in classical power converters (rectifiers and hard-switching power converters) [7].

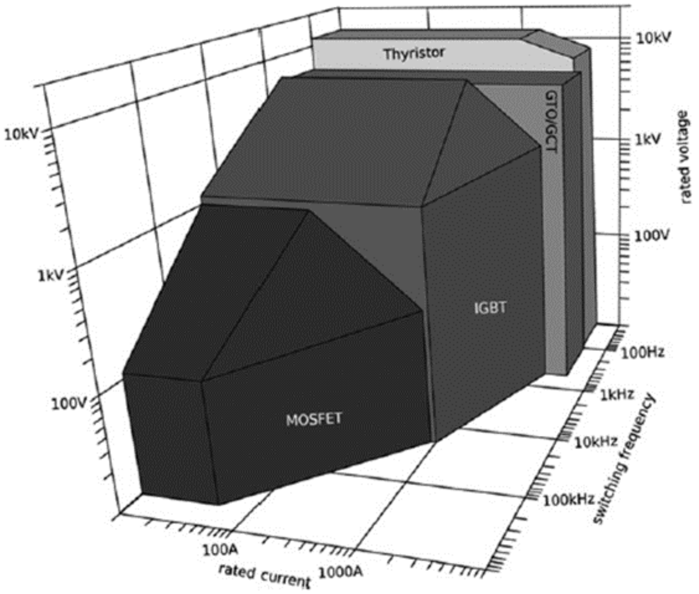


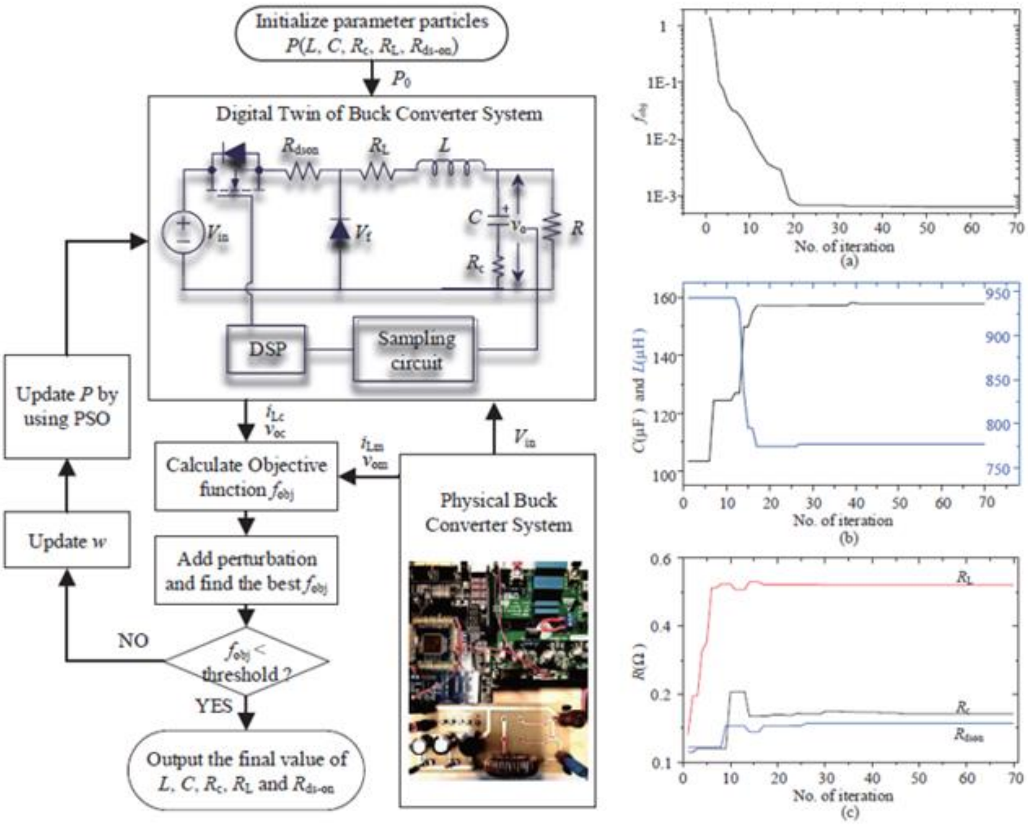
Figure 4: Operation range of silicon power semiconductor devices [7]

2.2.2 Digital twin modelling of power devices

Reliability analysis of power electronic components has posed a significant challenge since their initial deployment. Sh. Yang et al [8] conducted a comprehensive and extensive survey by sending questionnaires to various experts, inquiring about the reliability requirements of power electronic applications. The feedback they received indicated that in over 70% of the responses, the failure of power semiconductors was a prevalent issue, with capacitors being identified as the second cause of failure in power converters in 46% of the responses. Hence, the implementation of a monitoring system is imperative to prevent unforeseen failures. However, condition monitoring, through the application of measurement devices, is a well-established methodology for assessing semiconductors. As an illustrative example, in [9], an aging test was conducted on three Insulated Gate Bipolar Transistors (IGBT) manufactured by three different companies (IR Electronics, Fuji, IXYS). This test employed a thermoelectrical degradation process to evaluate the impact of manufacturing uncertainties on the lifetime of these devices. To facilitate this test and for monitoring purposes, they employed highly accurate measurement devices and integrated designed circuits to monitor various variables of the IGBT, including case temperature, gate current, gate voltage, collector current, and collector-emitter voltage, with distinct sampling windows. Their results demonstrate the reliability of these methods. However, it's important to note that when discussing monitoring, it involves the continuous acquisition of measurements over time. Consequently, there is a risk that not only may the added measurement devices or sensors degrade over time, but also introducing new circuits and components into the primary design may prove challenging. An example of such devices can be found in [10], where an advanced testbed has been developed for simultaneously monitoring the on-state resistance and case temperature of multiple discrete power MOSFETs under cyclic electro-thermal tests. Similar examples of the application of these methods can be found in the literature. To address this issue, the use of the digital twin model can provide a solution. Depending on the type of problem and the physical model there are different methodologies for creating a digital twin, as explained in [11]. In this context, two of the most commonly applied methods in the area of power electronics have been elaborated in detail and the problem of uncertainty in these models is discussed.

Physics-based digital twinning

The most critical aspect of creating a digital twin is the modelling of the physical space. The physics-based modelling method involves modelling the real world based on physics concepts. As an example of this concept, Y. Peng et al [12] introduced a non-invasive methodology for creating a digital twin model to simulate DC-DC power converters without the need for additional devices in the circuit. In their research, they developed a digital twin of a buck converter and estimated its parameters using the Particle Swarm Optimization algorithm (PSO). Furthermore, they added a few components to the model to simplify the differential equations (sampling circuit and DSP).



a) b)

Figure 5: Digital twin algorithm and the results [12]

In this method, the PSO algorithm is employed to compute the parameters of the digital twin model, including L, C, and R, by minimizing an objective function (Figure 5-a). To validate their approach, they conducted experimental tests. It can be observed from Figure 5-b that after 50 iterations, the objective function was minimized, and the model's parameters stabilized. Several similar studies in this field exist. For example, in [13], they utilized MATLAB Simulink to solve the model's equations. In [14], NI LabVIEW was used to solve the equations of a DC-DC Boost converter, and in both cases, PSO was applied to estimate parameters. Furthermore, in [15], the Genetic Algorithm (GA) optimization method was used instead of PSO, and it was demonstrated that the application of GA led to a faster minimization of the objective function (more similar works in [16,17,18,19,20,21]). Model-based approaches can also be valuable for constructing a digital twin model aimed at analysing the thermal performance of power semiconductors. B. Rodrigues et al [22,23] introduced a method for creating a thermal digital twin of power devices. In their approach, they utilize a simplified Lumped Parameter Thermal Network (LMPTN) to model the thermal profile of the component, and they've enhanced the model's capability to predict the thermal parameters of the device by employing the Kalman filter. However, these methods require the use of a few thermal sensors (also refer to [24], where PSO is employed to estimate the parameters of a Cauer model).

Additionally, the Finite Element Method (FEM) is another method for physics-based modelling. S. Race et al [25] introduced a methodology for optimizing the design of the board test for characterizing power electronic switching cells. They modelled the switching cells using the mixed-mode simulation methodology as explained in [26,27], and they redesigned the measurement board based on engineering judgment to minimize the error between the output of the Double Pulse Test (DPT) applied in FEM and the real element.

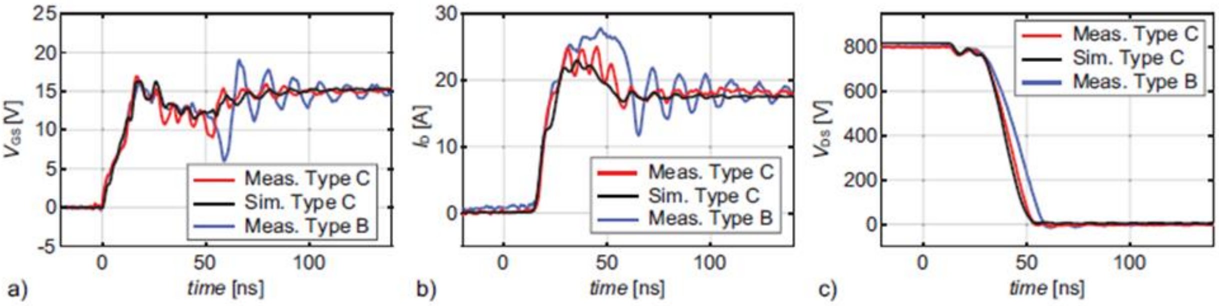


Figure 6: Type B: before the change, Type C after the change [25]

Similar to the aforementioned research, in [28], the physical element was substituted with a high-accuracy Finite Element Model (FEM). This model was employed to estimate the parameters of both the circuit model and thermal model (Cauer model) of a digital twin of a DC-DC boost converter.

Machine Learning (ML)-based digital twin modelling.

In recent years, the application of Artificial Intelligence (AI) in various research domains, including the reliability analysis of microelectronic devices, has increased. A comprehensive review of the application of these methods can be found in [29], where six different ML models, including Artificial Neural Network (ANN), Recurrent Neural Network (RNN), Support Vector Regression (SVR), Kernel Ridge Regression (KRR), K-Nearest Neighbour (KNN), and Random Forest (RF), were trained using data generated by a Finite Element Model (FEM) to lifetime prediction of five different test vehicles' Wafer Level Packaging (WLP). They used the thickness of the silicon chip, stress buffer layer, upper pad diameter, and lower pad diameter as inputs for their model, and they simulated various thermal loading conditions. This data was used to create an ML model for predicting the reliability life cycle. The results indicate that the ANN method achieves better accuracy than the others, although the computational cost is higher than that of the other methods.

Furthermore, ML methods can be applied for fault classification in power electronics, as demonstrated in [30], where an ANN model is trained for fault classification in the time domain, aided by the Discrete Wavelet Transformation (DWT) methodology for feature extraction. In a similar study, H. Krishnamoorthy et al[31] utilized MATLAB Simulink to simulate a boost converter and employed this simulation to generate the necessary data for training an ML model to estimate the time domain response of the load voltage. To achieve a high level of accuracy in estimating the current ripple, they utilized the Bayesian Regularized ANN (BR-ANN) model to address the issue of overfitting. Furthermore, although their results demonstrate the strong performance of BR-ANN in terms of tracking the peak overshot, settling time, and the steady average value of power converters under various conditions, they also recommend using RF to accurately capture the steady-state ripple.

In all of the cases mentioned so far, static data has been used to train the model, meaning that the output remains fixed at any instant for fixed sets of input. Nevertheless, a digital twin must be general enough to capture all potential operating modes and conditions to which the physical twin will be subjected. On the other hand, collecting enough data from the real operational conditions of the device can be challenging. For instance, in the research presented in [32] for monitoring a power converter in a wind turbine application, it took two and a half years to collect enough reliable data. Although, one solution could be the application of Physics-Informed Machine Learning

(PIML), results in [33] indicate that elements highly affected by operational conditions like temperature, current, etc., may exhibit a high level of variation since these factors may not be applied in the physical model of the device.

To address this limitation, A. Wunderlich et al [34] present a method for creating a digital twin of power converters through the application of a dynamic ANN called Nonlinear Auto Regression Exogenous ANN (NARX-ANN). It contains memory blocks that enable it to replicate systems of differential equations, specifically the nonlinear state equations of a power converter. They utilized this method to establish a link between the input voltage and duty cycle of the input load and the inductor current and capacitor voltage of a boost converter.

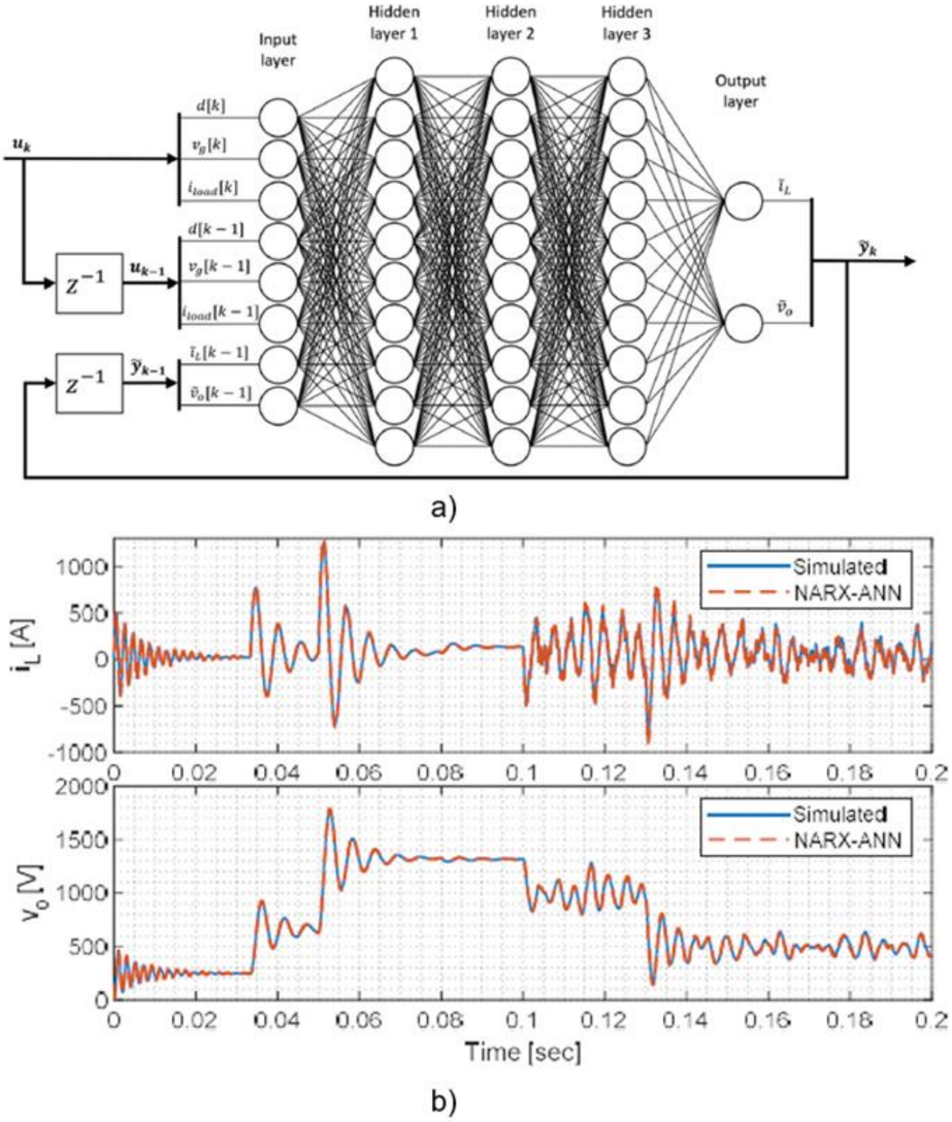


Figure 7: NARX-ANN algorithm and the results [34]

The model is implemented in MATLAB, and a network is trained with a dataset comprising a combination of large amplitude chirp signals, low-frequency sinusoids, step functions, and white noise. As shown in Figure 7, the results demonstrate the excellent performance of NARX-ANN in predicting both steady-state solutions and a wide range of transient conditions and wideband perturbations.

2.2.3 Uncertainty quantification in digital twins

As previously mentioned, a digital twin is a probabilistic simulation of the physical element. This probabilistic nature arises from various sources of uncertainty, including EMI, thermal effects, component tolerances, manufacturing defects, fluctuating loads, and others. M. Milton et al[35] introduced a method for creating a probabilistic digital twin using the Polynomial Chaos Expansion (PCE) probabilistic modelling approach. Their work employs a simplified PCE not only to calculate the parameters of the equivalent circuit (such as the calculation of L, C, and R in a buck converter) but also to estimate their associated uncertainty. Through an iterative procedure, the expected output value of the digital twin (e.g., current or voltage) and its mean absolute deviation, are compared to the output of the physical system. Abnormality in the physical element is defined when the measured value falls outside a defined threshold range, defined as the mean expected value plus and minus the mean absolute deviation.

In another study, in [36], the Bayesian optimization approach was utilized to determine the best subsequent samples for identifying the parameters of the circuit model of a buck converter, with the goal of minimizing the discrepancy between the output of the digital twin and the real model (e.g., inductance current and output voltage). They compared their proposed method with PSO and demonstrated that in their approach, the objective function can be minimized more rapidly (see also [37,38,39]).

2.2.4 Conclusion

As mentioned earlier, a digital twin is a virtual real-time representation of a physical element. However, as it is well-stated that "in principle, all the simulation results are wrong unless one can prove that they are right", various methods have been suggested to enhance the accuracy of the virtual model, as seen in [12], [25] or [34]. However, in the proposed methods in [12], after any change in the physical model, the parameters of the twin need to be updated again to minimize the objective function. In the method proposed in [25], it is evident that the modelling itself is complex, and updating it in iterations would be time-consuming; therefore, these two methods are not real-time digital models. Furthermore, although the method proposed in [34] predicts the time-domain response of the device, it is not able to detect and classify abnormalities in the model's output. Hence, the development of a new real-time digital twin model with the ability to classify faults in the device based on the detection of abnormal performance is recommended in this study.

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2.3 DC6 Reliability of IC packages under small loading conditions

2.3.1 Introduction

IC Packaging is a kind of protective shielding for semiconductor chips. This protective layer not only provides a shield to components but also protects it from any environmental and mechanical stress. It also helps to develop electrical connections with the external circuits [1]. For thermal management [2], IC packaging dissipates heat generated during operations. IC packaging plays a vital role in making circuits compact known as the miniaturization of ICs. Customization can also be done in accordance with specific requirements.

Understanding of failure modes are very pivotal for ensuring the reliability of electronic equipment and devices. If the possible failures are recognized earlier that will help in improvements in design optimizations that will result in higher product quality. If the failures are addressed actively then the risk of any product malfunction and product costs are reduced significantly. If the failure modes are analysed carefully and the appropriate countermeasures are taken with the time that will enhance the product quality for customer satisfaction [3].

The review is carried out on IC Packaging to evaluate its design and performance. The evaluation includes its capabilities of being electrical, thermal and suitability for various applications. It involves different pros and cons and advancements in the field. The review structure is based on highlighting significance of IC Packaging and its behaviour under the loading conditions.

2.3.2 Types of IC Packaging and Materials

There are various types of IC Packaging can be seen in the Figure 8 [4]. A dual inline package (DIP) is one of the immediate package types it is categorized by two parallel rows of pins for a through-hole mounting on a PCB. A Quad flat package (QFP) is the square body of pins on all four sides, it optimizes space on the PCB. A ball grid array (BGA) is like an array of solder balls for electrical connections by enhancing electrical and thermal performances. Chip scale package (CSP) is a very compact package itself. CSP is an Ideal for miniaturized devices. Package types like Small Integrated Circuits (SOIC) and Thin Small Outline Packages (TSOP) are used to cater to industrial needs with the consideration of factors like size, power, and thermal dissipation [5]–[8].

The packaging material also has a substantial value with respect to heat dissipation, dependability, and the electrical performance of the IC. This includes the choice of materials used for inside the packaging such as solder alloys, substrate, underfill compound, and die attach materials because they have the key impact on semiconductors performance regarding thermal management, inside electrical connection, and mechanical integrity. That is why an appropriate selection of materials is highly concern, which can give you surety for the product's long life and operational strength [5].

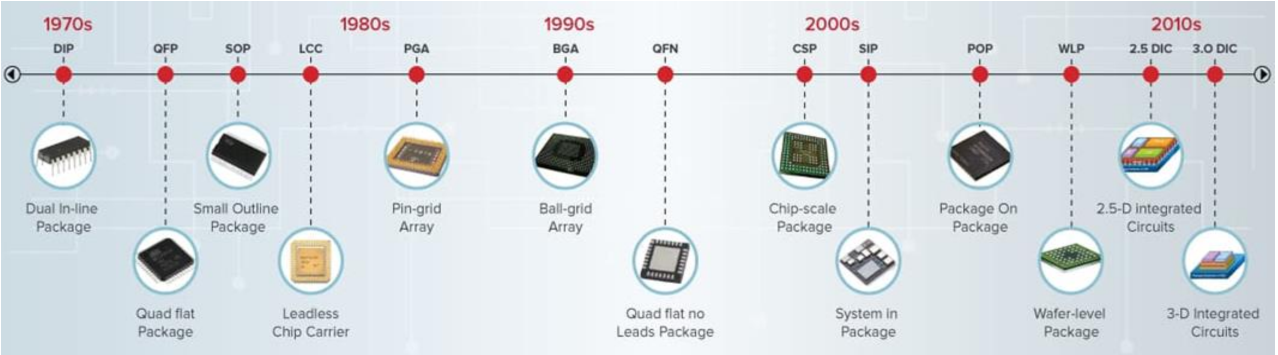

Figure 8 History of IC Packages [4]

2.3.3 Failure Modes Associated with IC Packaging

These five fundamental failure modes are the basis for all other observed failure conditions. These modes provide the framework for comprehending and dealing with different types of failures. These five modes of failure identification and classification help us better assess and reduce possible risks [9]. In order to create successful prevention and resolution strategies, it is imperative to comprehend the underlying causes of failure.

- Thermal-related failure modes (e.g., thermal fatigue, thermal overload).
- Mechanical-related failure modes (e.g., mechanical shock, bending, vibration).
- Environmental factors (e.g., moisture and humidity, chemical contamination).
- Voltage and ESD-related stress and failures.
- Electromigration and electrical failures.

Thermal-Related Failure Modes

Electronic device malfunctions related to heat stress arise when a disproportionate amount of heat negatively impacts the dependability and efficiency of individual parts. Thermal overstress, which occurs when semiconductors have been subjected to excessive temperatures for an extended period of time and surpass their designated operating limits, is a common thermal-related failure that can result in permanent damage or decreased efficiency [10].

Thermal cycling is yet another issue. This occurs when there are frequent changes in temperature, which puts mechanical stress and fatigue on solder joints and packaging materials in particular. Eventually, this leads to cracks and electrical discontinuities that can be seen in Figure 9 [9].

Electromigration, the process where metal atoms relocate through pathways of conductivity to create open circuits or shorts, can also be accelerated by overheating. efficient thermal layout, dissipating heat approaches, and tracking of temperature are crucial factors to take into account when designing and producing electronic systems in order to reduce thermal-related failures.

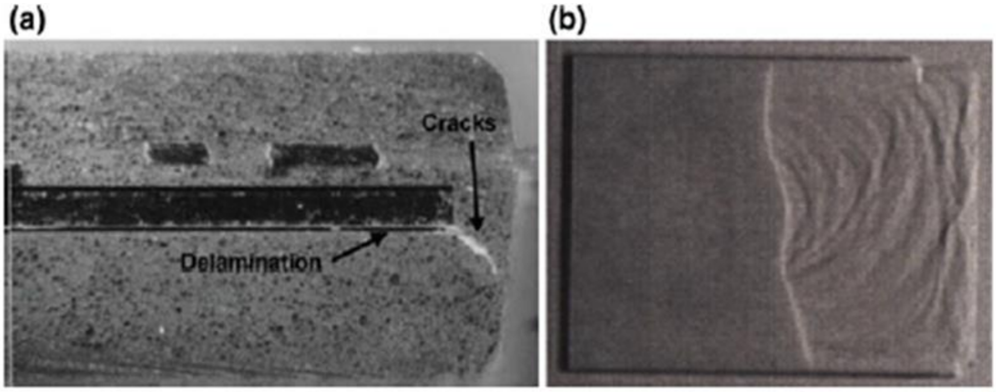

Figure 9 (a) Solder Fatigue, (b) Cracks on Substrate

Mechanical-Related Failure Modes

Mechanical-related failure modes encompass a range of potential issues, including mechanical shock, bending, and vibration. Mechanical shock is the most common one which occurs due to mishandling or during the transportation of the device which results in package crack, wire bond failure, and fractures in solder joints. These fatigues can easily cause the device to malfunction. Bending stress [11], which can cause mechanical cripple, and delamination inside the package, can be brought on by PCB bending or inappropriate installation.

Vibration, which is experienced in a variety of applications, can lead to structural fatigue, which can cause package degradation over time, loose connections, and poor electrical performance. To reduce these mechanical-based failure modes and ensure the resilience of semiconductor devices, rugged package design, and cautious carrying are necessary [12].

Environmental-Related Failure Modes

The failure modes of IC packages are significantly influenced by environmental variables. The package may become moist or humid, which can lead to electrical short circuits, oxidation, corrosion, and other problems. Additionally, package materials may deteriorate due to chemical contamination from exposure to pollutants or reactive substances, which could result in fatigue cracks and debilitated electrical connections. It is essential to secure IC packages from these atmospheric conditions through appropriate seal-off, and conformal coatings, in compliance with industrial benchmarks.

Voltage and ESD-Related Stress and Failure Modes

For integrated circuit (IC) packages, voltage and stress caused by electrostatic discharge (ESD) are the main sources of worry. Excessive voltage conditions, whether brought on by power surges or precipitous spikes, can cause gate oxide damage, dielectric breakdown, and even irreversible device breakdown. The small components within the IC packages are also at risk from ESD events, which are characterized by quick and high-voltage discharges. These voltage discharges have a substantial negative impact on the functioning and dependability of ICs, including gate oxide breakdown and damage to the junction. To protect IC packages from voltage and ESD-related failures and preserve their working reliability, effective ESD protection arrangements, such as semiconductor diode and applicable layout models, are mandatory.

Electromigration and Electrical Failures Modes

Electromigration and electrical failures also challenge the IC packages with respect to their reliability. High current density-driven electromigration can gradually displace material within conductive paths, increasing resistance, changing electrical properties, and potentially causing open or short circuits. The efficiency and long-term constancy of ICs can also be distressed by electrical failures like dielectric breakdown, and gate oxide damage [13]. To address these problems, ensure the stable performance of semiconductor devices and prevent electrical deterioration in the long run, careful material picking, accurate manufacturing methods, and cautious voltage control are vital.

Competing Failure Modes

Competing failure modes describe the state in which multiple failure modes interact with one another within a system or component, possibly impacting or speeding up the occurrence of each other. Stated in various ways, competing failure modes entail the interaction or interdependence of various failure mechanisms [14]. Further clarification on the competing modes has been presented by Gerald et al [15]. The test was conducted in strain control at a higher temperature via a nickel alloy material. Recorded are two separate failure sites It can be seen that surface-initiated failures are observed at high stress levels, whereas internal and surface-initiated failures coexist at intermediate stresses and internal initiated failures predominate at lower stress levels.

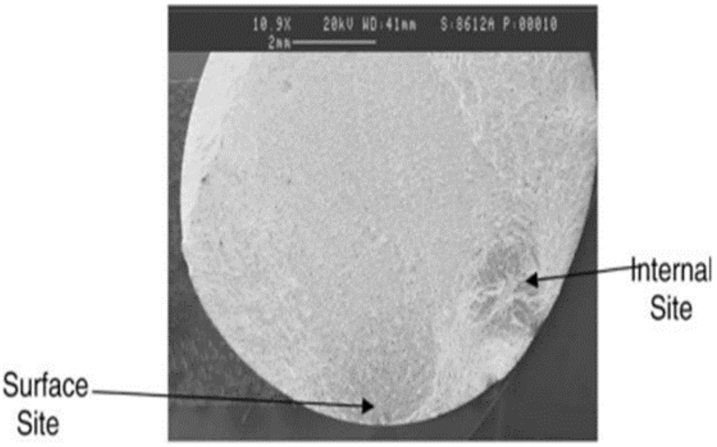

Figure 10 Fatigue fracture surface demonstrating competing surface and internal initiation sites [10]

2.3.4 Mitigation and Reliability Enhancement Strategies

There are four encompassing strategies that are required to reduce risks and improve the reliability of integrated circuit packages which are listed below:

- The first one is to strengthen the design constraints such as solid ESD safety, efficient heat dissipation method, and improved Layouts are necessary [16].
- Second, depends on the selection of materials such as top-quality die electrics, appropriate substrate, and dependable solder alloys perform key aspects.
- Third is the testing and qualification procedures which adapt accelerated life testing (ALT) consisting of temperature cycling and humidity testing [17], and failure analysis techniques like x-ray analysis for finding the initial cause of breakdown.
- The fourth one is the reliability engineering techniques namely, the design of experiments (DOE), Weibull assessment, and quality function deployment (QFD). DOE makes it possible to systematically enhance and authenticate the design parameters. Weibull technique is used to assist in failure rate forecasting and design flaw detection. However, QFD coordinates in upgrading the design features with customer requirements.

Semiconductor companies can enhance the quality of IC packages while minimizing failure modes through the implementation of these approaches and standard procedures, which will ultimately result in the delivery of reliable and long-lasting electronic components and devices to the consumer.

2.3.5 Conclusion

In this review, we examined at the most significant strategies and techniques for reducing risks and improving IC (integrated circuit) package reliability. In a technological environment that is constantly changing to satisfy the high reliability needs of contemporary applications and sectors, the awareness and control of competing failure modes become crucial to ensuring the continued advancement of semiconductor technology.

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2.4 DC10 Microstructure Informed Modelling and AI for Reliability Predictions

2.4.1 Introduction

The assurance of reliability performance of solder joints is an important consideration in electronic packaging and comprehending the factors that affect it is essential for the design and performance of electronic devices. For solder joints, degradation and failure due to thermal fatigue as a result of thermally induced stresses caused by the coefficient of thermal expansion (CTE) difference of the materials in the assembly (CTE mismatch phenomenon) is the main challenge. The principal causes of failure are the alternating strains and stresses resulting from thermal expansion mismatches. This review also investigates the influence of solder joint geometry, with a particular focus on the significance of factors such as form, standoff height, and the use of various techniques such as stacked solder and double bump technology.

The flexible printed circuit board (FPCB) is known for its unique characteristics, such as its ability to withstand vibrations, enhanced flexibility, and reduced thickness. These characteristics are crucial for achieving miniaturisation and replacing rigid boards. The key factors that determine the dependability of solder junctions are their form and standoff height.

The review also examines various inelastic (visco-plastic) material models, such as the Norton-Hoff, Perzyna, Chaboche, Bodner-Partom, Anand, and Johnson-Cook models. The need of employing thermo-mechanical damage modelling at microstructure level, for example using crystal plasticity model, for Sn-based Pb-free solders is underscored, taking into account aspects such as heat activation and back stresses.

2.4.2 Solder joints shapes

Alternating strains and stresses generated by the mismatch in the coefficient of thermal expansion of the electronics component/assembly materials are the main causes of failure in solder joint interconnections. Several aspects have been identified to be affecting the solder joint reliability, such as solder joint shape, board material, chip size, interface metallurgy, and underfill and substrate materials. The distinctive properties of the flexible printed circuit board (FPCB) include vibration resistance, increased flexibility, and decreased board thickness. That because of its small weight and flexibility, FPCB is essential in miniaturisation of electronics products and replacement of rigid boards (RPCB). The primary determinant of solder joint reliability is the shape and standoff height of the solder joint geometry. Various methodologies have been documented in the literature to enhance the standoff height and regulate the configuration of solder bump connections. These include stacked solder, double bump technology, stretched solder, ceramic column grid array, and the second-reflow-process approach. The stacked solder approach employs the utilisation of bump-limiting metal pads to facilitate the separation of solder bumps at various levels through a sequential stacking procedure. The double bump technology refers to the deliberate and controlled overlaying of two molten solder bumps on the surfaces of two components, resulting in the formation of a connection that is practically cylindrical in shape. The utilisation of a mechanical standoff was employed in this methodology to regulate the ultimate distance between packages and printed circuit board (PCB). One method for achieving a cost-effective stretch solder joint is by stretching the solder joint to provide an hourglass shape and increased standoff height. Solders with an hourglass form exhibited the lowest plastic strain and demonstrated enhanced dependability when subjected to thermal cycling. Among solder joints with a fixed solder volume and pad size, it was observed that the hourglass-shaped solder joint exhibited the highest standoff height, while the column and barrel shaped solder joints followed suit in descending order.

2.4.3 Various Solder Joints geometry

The geometric characteristics of the solder joints are quantified using two dimensionless factors, namely the aspect ratio (AR) and the form factor (SF) [1]. These parameters are mathematically defined as follows:

$$\text{Aspect Ratio (AR)} = \frac{H}{D} \quad (1)$$

$$\text{Shape Factor (SF)} = \frac{M}{D} \quad (2)$$

In this context, H represents the vertical distance between the solder joint and the surface it is attached to. D denotes the diameter of the pad, while M refers to the diameter at the midpoint of the solder joint. The term "SF" is commonly used to refer to the solder joint's profile as shpwn in Figure 11.

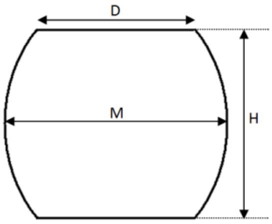

Figure 11: Barrel Shape Solder Joint with Specifications.

Volume of barrel shaped solder joint (V_T) is given by

$$V_T = \frac{\pi H}{12}(2M^2 + D^2) \quad (3)$$

Then the value of H for the remaining geometries are determined by applying the truncated ellipsoid model as indicated in Eq. (4) and these geometries are represented in Figure 12.

$$H = \frac{15\, V_T}{\pi(2M^2 + MD + 0.75D^2)} \quad (4)$$

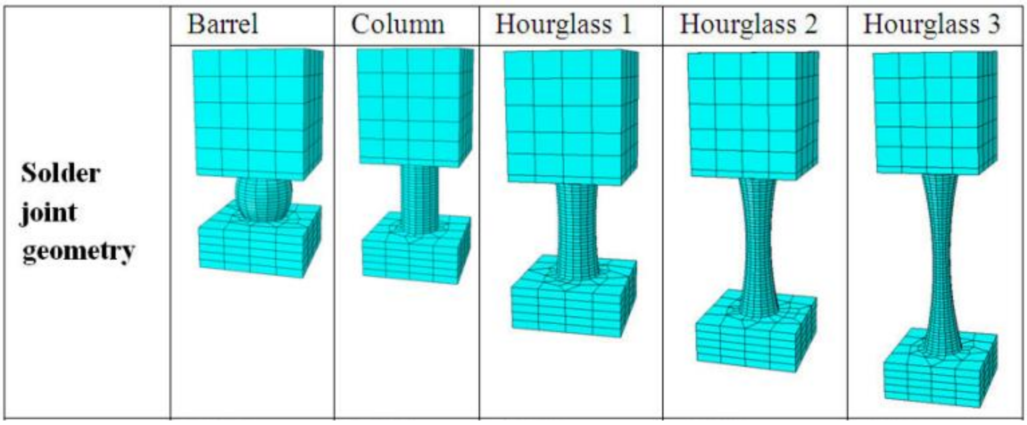

Figure 12 Various Solder Joint Geometries with Specifications [2]

2.4.4 Accumulated inelastic strain

In thermo-mechanical analysis of solder joints using finite element method, the thermal fatigue damage is commonly evaluated using the inelastic (visco-plastic, creep) strain or strain energy density accumulated over a temperature cycle with a stabilised hysteresis loop. For a component assembled on a printed circuit board, the distance of the joint from the neutral point of the package is one factor that dictates the level of damage under temperature cycling. In the case of RPCB, the joints of ball grid array components with critical functional performance are commonly located at the inner rows, as shown in Figure 13, because these joints, being closer to the neutral point of the package, are less prone to the effects of the CTE miss-match stressing. In FPCB, the damage susceptibility of joints, location-wise, vary and is also impacted by the shape of the joints. Increasing the aspect ratio causes the crack locations in solder joints on RPCB to move from the chip-solder interface to the midpoint of the solder joint.

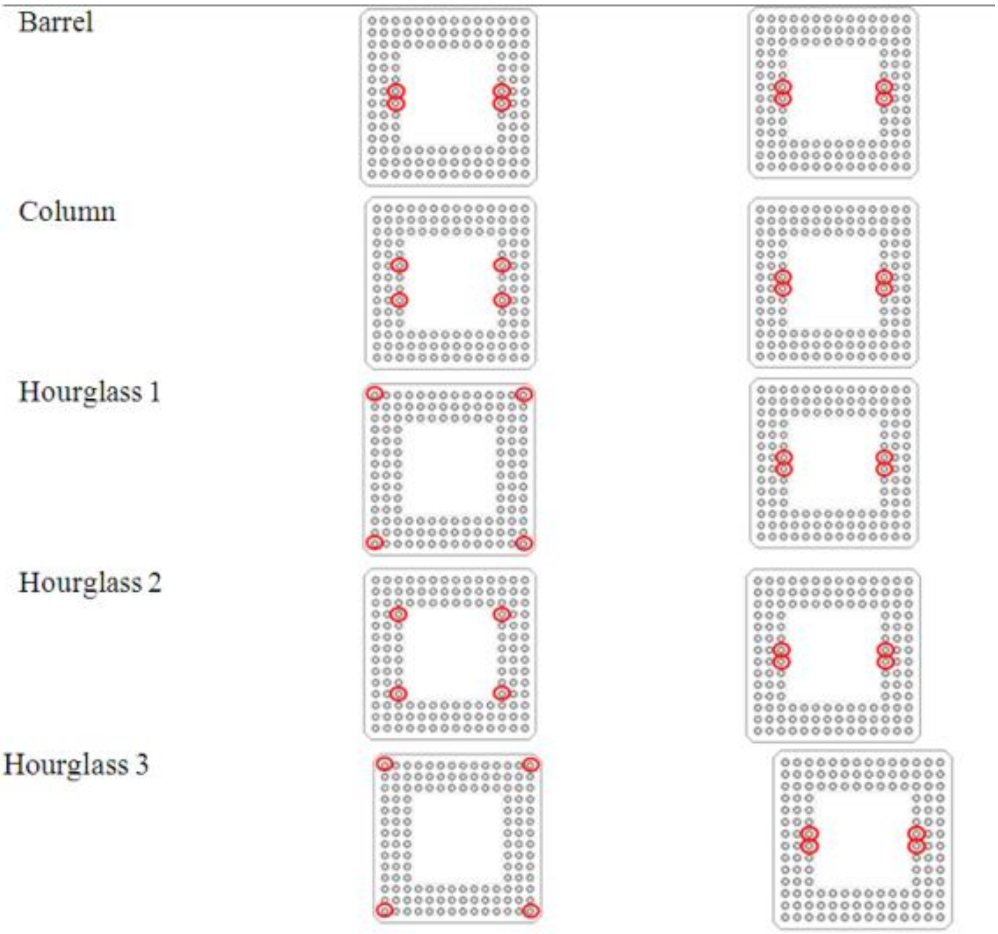

Figure 13 Typical locations of Critically Affected Solder Joints on FPCB and RPCB [2]

2.4.5 Crystal plasticity model for Visco-plastic Mechanical behaviour

Electronic products undergo temperature cycling caused by power and environmental cycling throughout their operation. Thermal cycling creates thermo-mechanical stress in solder junctions due to the varying coefficients of thermal expansion (CTEs) among the packaging materials. Solder joints are also exposed to external impact forces, such as vibrations and shocks. The solder joints in electronic packaging materials are the most susceptible to failure due to the low strength of these materials. Thermal fatigue of solder connections occurs when thermal stress causes the solder joint to distort and accumulate permanent damage, leading to a failure mode in the form of crack that can be at either the package or at the substrate side of the joint. Hence, the study of thermo-mechanical fatigue (TMF) in solder alloys has gained significance in the process of optimising the design of solder joint interconnections [3].

Neu [4] examined the stress-strain hysteresis behaviour of 96Sn-4Ag and Castin (96.2Sn-2.5Ag-0.8Cu-0.5Sb) solder when subjected to thermo-mechanical coupling between 218 and 398 K. Similarly, research was also carried out on the increasing strain evolution behaviour of SAC305 solder under thermo-mechanical coupling between 333 and 373 K.

The primary constituent of Pb-free solder based on Sn is β-Sn, which possesses a body-centred tetragonal (BCT) structure with several slip systems and an orthotropic elastic constant and coefficient of thermal expansion (CTE) [5]. A typical solder junction often consists of a small number of big grains that have comparable orientations. The differences in properties between these crystals are more noticeable. Hence, it is imperative to examine the anisotropy through the lens of crystallography, specifically with the crystal plasticity approach. Nevertheless, there is a scarcity of research on the anisotropy of solder when subjected to thermo-mechanical coupled loading.

There are two distinct types of thermo-mechanical crystal plasticity models available for metals and alloys. One type of analysis, suitable for material processing or uniaxial deformation, does not take into account the response of the cyclic stress-strain hysteresis loop [6]. The other type of analysis considers TMF and predicts the response of the stress-strain hysteresis loop [7]. However, there are only a limited number of thermo-mechanical crystal plasticity models that are appropriate for Sn-based Pb-free solders subjected to thermo-mechanical coupled loading. Dislocation density-based models have numerous parameters and are challenging to determine, while phenomenological models have a smaller number of parameters and possess comparable physical importance. Hence, it is necessary to create a thermo-mechanical crystal plasticity model for Sn-based Pb-free solders, taking into account the thermal activation, short-range and long-range back stresses of the macroscopic phenomenological unified creep-plasticity (UCP) model , thermo-mechanical crystal plasticity model needs to be formulated for Sn-based Pb-free solders [8].

The crystal plasticity models mentioned above are categorised and outlined in Table 1 based on their classification as either phenomenological or physical models, their incorporation of dislocation density, inclusion of thermal activation terms, and provision of definitions for back stress.

Table 1 Summary of the uses and types of some thermo-mechanical crystal plasticity models.

Author	**Application Processing**	**TMF**	**Model Type Phenomenological**	**Physical**	**Thermal Activation**	**Back Stresses**
Borkowski 2021 [9]	√			√	√	
Dong 2022 [10]		√	√			√
Dong 2016[7]		√		√	√	√
Meier 2014 [11]	√		√			
Ozturk 2016 [12]	√			√	√	√
Shenoy 2005 [13]		√	√		√	√

Note: In the rightmost two columns, the sign √ denotes the presence of this item

<u>Different type of inelastic material models for reliability</u>

1) **The Norton-Hoff Model:**

This model integrates both elastic and viscous constituents to highlight the time-dependent distortion of materials. It is commonly employed for forecasting creep behaviour.

2) **The Perzyna Model:**

The Perzyna model is renowned for its capacity to encompass the consequences of both elastic and inelastic deformations. It is commonly used to examine the visco-plastic properties of materials subjected to complex loading circumstances.

In the Perzyna model the evolution of the viscoplastic strain rate is defined as (Perzyna, 1966)

$$\dot{\boldsymbol{\varepsilon}}^{\mathrm{vp}} = \frac{\langle \phi(f) \rangle}{\eta}\mathbf{m}, \qquad (5)$$

with η the viscosity parameter, ϕ the overstress function that depends on the rate-independent yield surface $f(\boldsymbol{\sigma}, \boldsymbol{\Phi})$, and $\mathbf{m}$ given by equation .

$$\dot{\lambda} = \frac{\langle \phi(f) \rangle}{\eta}, \qquad (6)$$

where " $\langle\cdot\rangle$ " are the McCauley brackets, such that

$$\langle \phi(f) \rangle = \begin{cases} \phi(f) & \text{if } \phi(f) \geqslant 0, \\ 0 & \text{if } \phi(f) < 0. \end{cases}$$

The overstress function ϕ must fulfill the following conditions:

$\phi(f)$ is continuous in $[0, \infty\rangle$,
$\phi(f)$ is convex in $[0, \infty\rangle$,
$\phi(0) = 0$,

3) The Chaboche Model:

The Chaboche model is an expanded version of the Norton-Hoff model that is commonly employed for situations involving repeated loading. This model incorporates both isotropic and kinematic hardening and is utilised in the analysis of fatigue.

Chaboche model is described below

$$d\alpha = \sum \ d\alpha_i,\ d\alpha_i = \frac{2}{3} B_i d\varepsilon^p - \gamma_i \alpha_i \sqrt{\frac{2}{3} d\varepsilon^p d\varepsilon^p},\ i = 1,2,3 \qquad (7)$$

4) The Bodner-Partom Model:

This model is utilised for forecasting the creep and relaxation characteristics of metallic materials. This study takes into account the impacts of dislocation climb and glide in the process of deformation.

1) The Bodner-Partom (B-P) material model applied in simulations is based on three fundamental relationships :
   The plastic flow rule relates the inelastic strain rate $\dot{\varepsilon}_{ij}^{(ie)}$ with the deviatoric stress using the plastic multiplier .

$$\dot{\varepsilon}_{ij}^{(ie)} = \lambda s_{ij} \qquad (8)$$

where $\boldsymbol{s}_{ij}$ is deviatoric stress tensor (Eq. 10)

$$\boldsymbol{s}_{ij} = \boldsymbol{\sigma}_{ij} - \frac{1}{3} \boldsymbol{\sigma}_{kk} \delta_{ij} \qquad (9)$$

where δ_{ij} is Kronecker delta function.

2) The kinetic equation relates the plastic multiplier with the stress invariants using internal state variables.
3) The evolution law defines the changes of the internal state variables ($\dot{Z}^I$ and $\dot{\beta}_{ij}$).

5) Anand Model:

Solder exhibits visco-plasticity. Anand model is developed to integrate a visco-plastic constitutive relationship. The solder joint is considered as isotropic in the overall model, neglecting the influence of anisotropy produced by crystal orientations. The deformation resistance, which represents the time-independent plastic strain and time-dependent creep strain inside the material, is the only internal variable in the Anand model. It describes the features of material strain softening or hardening, temperature dependency, strain rate dependence. The Anand model is derived for experimental datasets of stress-strain curves obtained at different strain loading rates and at different temperatures. The model has nine constants which are determined by best fitting of the model prediction to the experimental data. The model is among the most widely used by the electronics packaging and assembly modelling community.

The constitutive equation of the Anand model is as follows:

$$\boldsymbol{\sigma} = cs,\ c < 1, \qquad (10)$$

Where c is a function of strain rate and temperature

$$c = \frac{1}{\xi}\sinh^{-1}\left\{\left[\frac{\dot{\varepsilon}_\mathrm{p}}{A_0}\exp\left(\frac{Q}{R_0 T}\right)\right]^{m_0}\right\}. \qquad (11)$$

The flow law and strengthening law equations are

$$\begin{gathered}\dot{\varepsilon}_\mathrm{p} = A_0\exp\left(-\frac{Q}{R_0 T}\right)\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m_0}},\\ \dot{s} = \left[h_{0,\mathrm{a}}\left(1-\frac{s}{s^*}\right)^{a}\operatorname{sign}\left(1-\frac{s}{s^*}\right)\right]\dot{\varepsilon}_\mathrm{p}, a > 1, \\ s^* = \hat{s}\left[\frac{\dot{\varepsilon}_\mathrm{p}}{A_0}\exp\left(\frac{Q}{R_0 T}\right)\right]^{n_0},\end{gathered} \qquad (12)$$

Where A_0(Pre-exponential factor), Q (activation energy), R_0 (gas constant), ξ (Stress multiplier), m_0, s^* (Saturation value of deformation resistance), n_0(Strain rate sensitive parameter of deformation resistance), $h_{0,\mathrm{a}}$(Hardening/softening constant), a (softening constants), and $\hat{s}$ (Initial value of deformation resistance) are Anand constitutive model parameters.

6) **The Johnson-Cook Model:**

The Johnson-Cook model, initially designed for high-temperature scenarios, is also employed to simulate the visco-plastic response of materials experiencing significant strain rates.

Using the Johnson-Cook model, the flow stress can be expressed as:

$$\sigma = \underbrace{(A + B\varepsilon^n)}_{\text{Elasto-Plastic term}}\ \underbrace{\left[1 + C\ln\left(\frac{\dot{\varepsilon}}{\dot{\varepsilon}_0}\right)\right]}_{\text{Viscosity term}}\underbrace{\left[1-\left(\frac{T-T_\text{room}}{T_\text{melt}-T_\text{room}}\right)^{m}\right]}_{\text{Thermal softening term}} \qquad (13)$$

7) **Visco-plasticity Model with Unified Formulation:**

Several scholars provide integrated models that seek to encompass a broad spectrum of material behaviours under different loading conditions. These models aim to offer a thorough depiction of visco-plasticity.

Microstructure of solder joints

The microstructure of solder joints pertains to the intricate organization and properties of the solder substance on a microscopic scale. This includes characteristics such as the dispersion of intermetallic compounds (IMCs), the arrangement of grains, and any alterations arising from particular treatments or procedures. An essential aspect in comprehending the characteristics of the solder connection, such as its strength, dependability, and resistance to elements like temperature and mechanical stress, is the examination of its microstructure.

Various researches have been performed to investigate the microstructure of solder joints. Figure 14 illustrates solder joints subjected to different durations of ultrasonic treatment. The thickness of the Cu6Sn5 intermetallic compound (IMC) layer first lowers, becomes more uniform after 10 seconds of treatment, and subsequently thickens due to excessive treatment, leading to a decrease in mechanical properties [14].

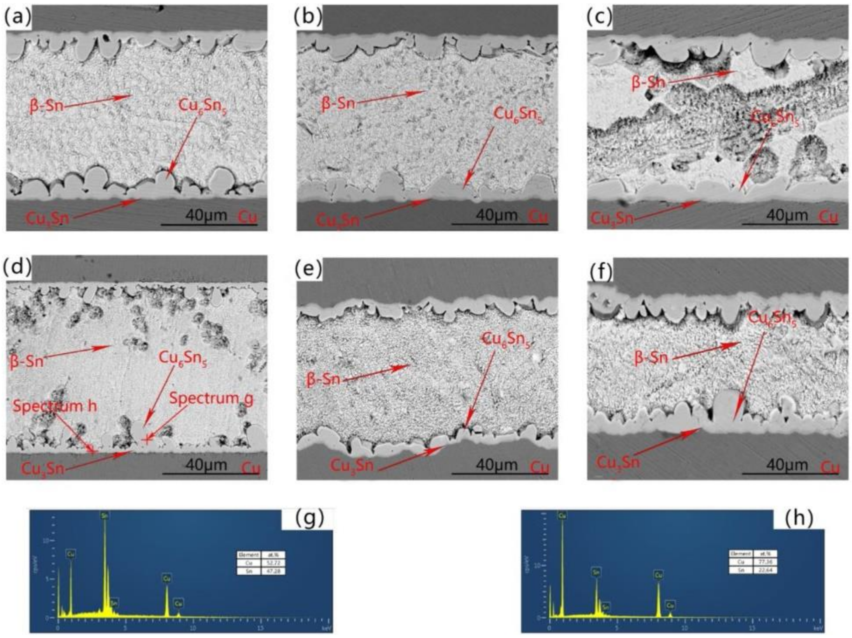

Figure 14 Microstructure at solder joint with ultrasonic treatment, (a) 0 s, (b) 1 s, (c) 5 s, (d) 10 s, (e) 15 s, (f) 30 s; (g-h) EDS analysis results.[14]

2.4.6 Common model assumptions

Finite element models of PBGA packages assembled on PCBs allow for the macro-scale analysis of solder joints, predicting the location of the most stressed joint, the level of damage and the damage interface within the joint. These models require having certain assumptions to simplify the calculation process and improve computational efficiency. These are as following:

1) The device is free from any process defects.
2) The residue stresses and strains resulting from device manufacturing should not be considered in this study.
3) All of the materials are linked together as perfect connections with de-bonding or any other issues ignored.
4) The electronic packaging devices dissipate heat very fast while the temperature undergoes slow variations resulting to quick conduction that can almost be considered a uniform temperature. For small balls in particular, the thermal transfer is quick with a minimal gradation of temperature. In light of that, it is made into a uniform temperature field disregarding the gradient of temperature.

2.4.7 Further research areas to cover in literature review

Under the DC10 project, literature review will be expanded in the following areas:

1) Thermo-mechanical fatigue in solder joints.
2) Comprehensive and methodical experimental investigation, specifically focusing on the temperature and strain phase, strain amplitude, and thermal cycle temperature range for solder.
3) Anisotropy in Sn-based Pb-free solder.

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2.5 DC12 AI-assisted design of high-performance and high-reliability probe technologies for EWS applications

Wafer probe test plays a crucial role to distinguish the good dies from the remaining defected dies on the wafers via the probe card as the testing signal interface between the tester and the integrated circuits on the fabricated wafers. Unexpected probe card failures that happen during the testing process will affect testing quality and reduce overall equipment efficiency and productivity. In practice, the engineers rely on domain knowledge and the process of trial and error for fault diagnosis and troubleshooting [1]. However, as the IC device features are continuously shrinking with an increasing number and density of the bond pads of the circuits on the wafer, fault diagnosis and troubleshooting for probe card have become complicated and time-consuming. To fill the gap, this study aims to develop an artificial intelligence assisted framework that integrates rough set theory and domain knowledge to derive effective decision rules to enhance the decision quality and efficiency for advanced quality control and smart manufacturing. The proposed framework can shorten fault diagnosis procedure and enhance productivity, while enhancing probing test integrity to reduce both the producer risk and customer risk. The developed solution will be implemented in real setting.

2.5.1 Probe Card Testing

Semiconductor products have become one of the most important components of various supply chains that leading countries have reemphasized the importance of semiconductor manufacturing (Chien et al., 2020b). Indeed, driven by Moore’s Law (Moore, 1965) that the number of transistors fabricated on a wafer will be doubled every 12 or 24 months, semiconductor industry has continuously migrated the technologies to shrink the feature size of the integrated circuit (IC). Thus, semiconductor industry is highly capital intensive, with complex and lengthy manufacturing process. In order to meet customer requirements and maintain competitive advantage, continuous yield enhancement for overall wafer effectiveness is critical for the semiconductor manufacturing companies (Chien & Hsu, 2014; Chien et al., 2013a, 2020a). In particular, wafer probe test plays a crucial role to distinguish the good dies from the remaining defected dies on each of the fabricated wafers that can reduce both the producer risk and customer risk via effective probing test. However, as the IC device features are continuously shrinking via technology migration, the fabrication processes as well as IC testing are increasingly complicated.

Semiconductor manufacturing consists of two phases for IC testing including circuit probing conducted on each fabricated wafer for sorting and final testing performed on the packaged IC (Hsu & Chien, 2007). The functionality and design specifications of each die can then be ensured by conducting IC testing. IC probe card is a crucial component as the signal interface between the tester and the tested wafers to detect failures against the designed electrical specification such as current, voltage, leakage, trigger and other functional speed as illustrated in Figure 15. To obtain reliable test results, the probe card that is characterized by a set of mechanical and electrical parameters should match with the tester and the devices to be tested such as device size and shape, the number of bond pads, and signal characteristics. Advanced quality control (AQC) is critical for yield enhancement in advance among the suppliers of semiconductor supply chain for virtual vertical integration to address the increasing challenges for maintaining technology migration for IC shrinkage (Chien et al., 2020a). Since probe card quality will affect the sensitivity and specificity of testing outcomes, it is important to enhance advanced quality control of the probe cards to ensure data integrity of IC probe testing results.

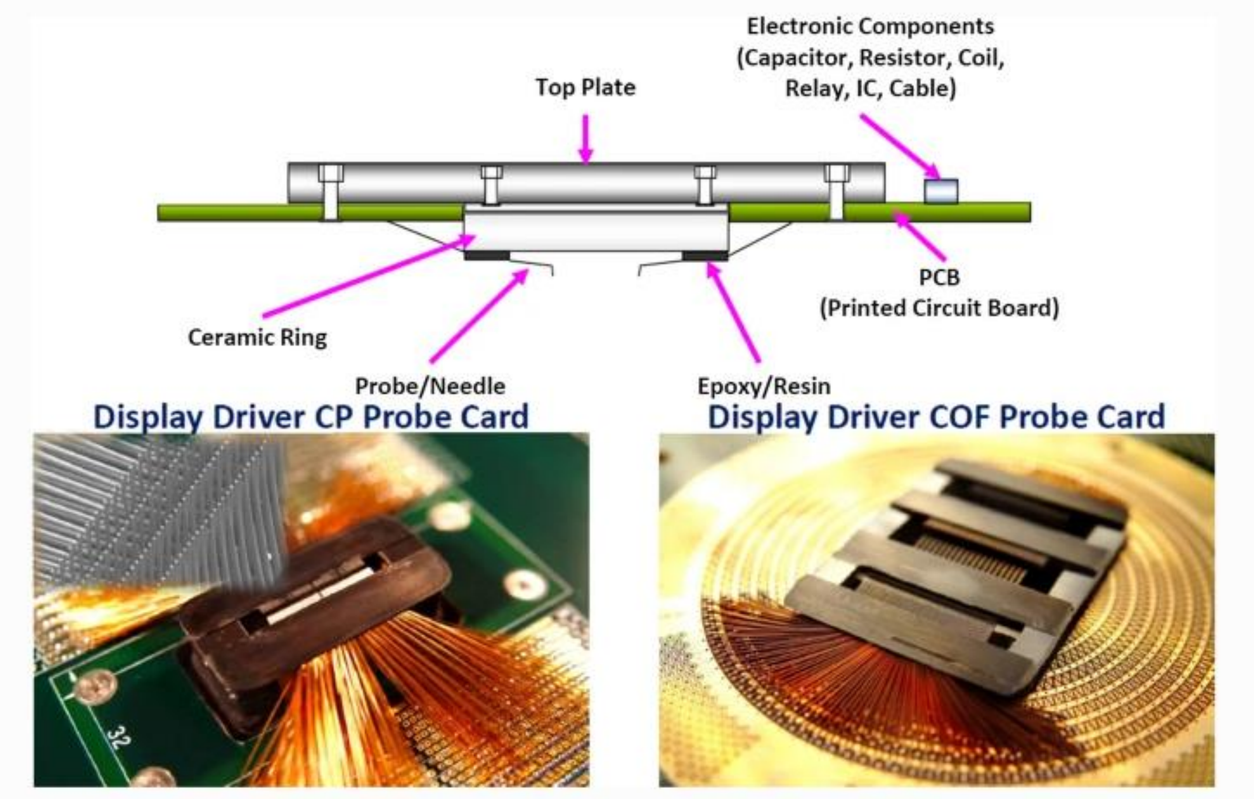

Figure 15: IC probe card and wafer probing test

In order to ensure IC quality and save packaging cost, semiconductor testing is an important process that involves the entire semiconductor supply chain. To ensure the produced wafers meet specifications, IC testing is performed to distinguish the good products from the defected ones. Each die on the fabricated wafer will be probing tested by the probe card of the tester to filter electrically dysfunctional dies. The testing results are shown as the wafer bin maps with spatial defect patterns for further diagnosis and yield enhancement (Chien et al., 2013b).

Probe card that serves as the mechanical and electrical signal interface between the wafer and testing equipment is a critical component of the wafer testing system, since probe card quality strongly influences IC yield rate. Misjudgement of specifications is not allowed, a stable and reliable contact interface is needed, and therefore high reliability of probe card is required in wafer testing. Figure 16 on the next page, illustrates the testing procedure for probe card.

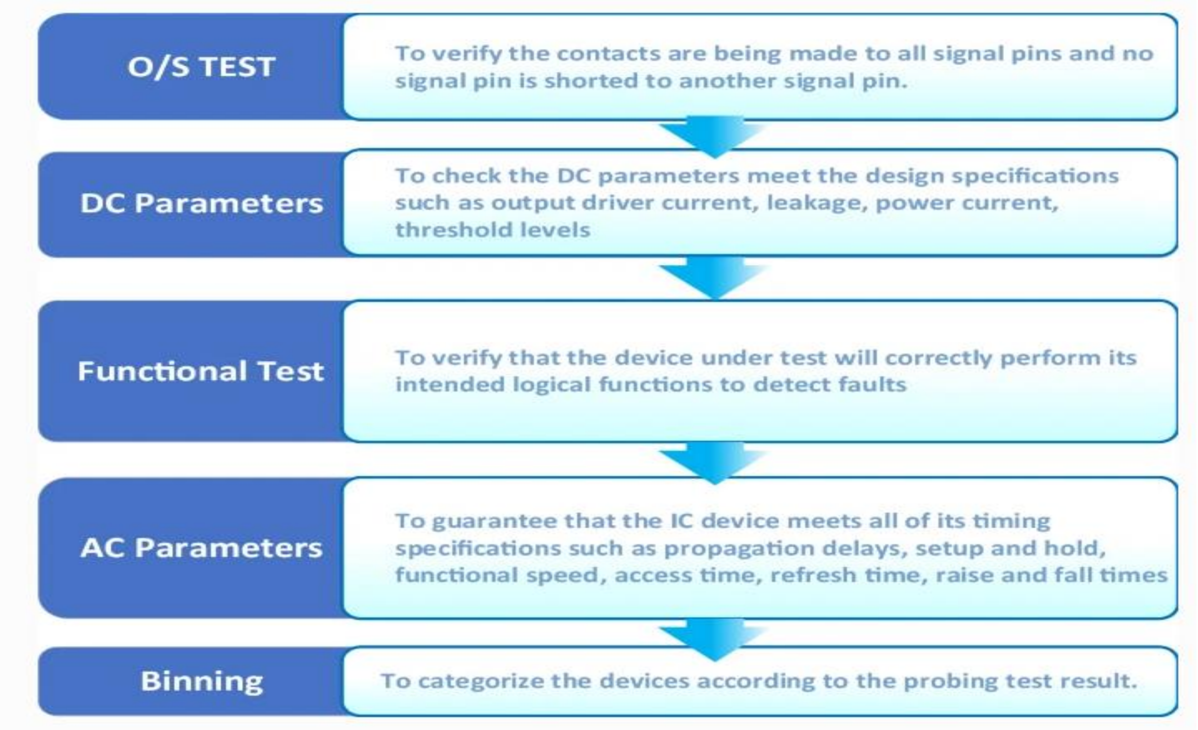

Figure 16: Probe card testing procedure

2.5.2 Rough Set Theory

RST is a data mining methodology to discover hidden patterns and derive useful decision rules under the incomplete or insufficient information (Pawlak, 1982). Different from conventional approaches, RST does not need to make the assumptions about the independence of variables and normality of data distribution (Chien et al., 2016). Furthermore, RST can deal with incomplete information for the present problem, while the "IF–THEN" rules derived by RST can provide simple and explainable information for the decision makers. Thus, RST is particularly suitable to support the engineers who should employ a series of steps to predict probe card parameters.

A number of studies have applied RST in various domains such as semiconductor manufacturing (Kusiak, 2001), printed circuit board manufacturing (Tseng et al., 2004), decision rule mining for machining method chains (Wang et al., 2022), and product feature design (Chien et al., 2014, 2016; Wu et al., 2020). In particular, Kusiak (2001) introduced rough set theory and data mining to extract effective decision rules from data sets for making predictions in the semiconductor industry. Chien et al. (2016) developed a data-driven framework based on RST to effectively extract product visual aesthetics and identify useful design concepts for product design. Wu et al. (2020) integrated rough set theory and information entropy to develop a knowledge recommender to enhance knowledge acquisition and reuse for new product development. Wang et al. (2022) developed a decomposition-reorganization approach for mining decision rules for machining method chains based RST.

Furthermore, RST has been applied for prediction in various areas including power system (Muralidharan & Sugumaran, 2013; Peng et al., 2004, 2017; Shen et al., 2000), medical diagnosis (Jothi & Inbarani, 2016), and image classification (Hassanien et al., 2009). Shen et al. (2000) applied RST in diagnosing the valve fault prediction for diesel engine and proposed a method suitable for discretizing the frequency and time domain attributes. Peng et al. (2004) used RST as a data mining tool for predicting fault diagnosis on distribution feeder, that useful patterns and rules are derived for faulty equipment diagnosis and fault location. Muralidharan and Sugumaran (2013) presented a rough set based rule generation and fuzzy classification of wavelet features for fault diagnosis of monoblock centrifugal pump. Peng et al. (2017) applied RST in fault diagnosis of different cable fault types by rejecting interference signals and recognizing partial discharge signals from different sources, and results showed that the proposed method have higher accuracy than SVM and Back-propagation Neural Network. Jothi and Inbarani (2016) presented a hybrid tolerance rough set and firefly based approach to classify MRI brain tumor image, that can select imperative features of brain tumor. Hassanien et al. (2009) presents a review of rough set and near set applications in medical imaging such as image segmentation, object extraction and image classification, while hybrid approaches including neural networks, particle swarm optimization, SVM, and fuzzy sets are discussed. Extensive review including extensions, theory and applications of RST can also be found, for example, in the research by Zhang et al. (2016). However, little research has been done in applying RST for probe card troubleshooting.

2.5.3 Structure Influence Relationship

In real settings, troubleshooting actions and procedures are different according to different product types and testing conditions. Based on domain knowledge, the influence relationship for probe card troubleshooting processes is structured. Due to the difficulty of collecting on-site testing data, engineers often diagnose the fault cases using the abnormal situation data and product information available. Thus, the abnormality situation and product information are two main factors that influence probe card testing. Experienced domain experts have their own AI models for frequently occurring abnormal situations, but the expert knowledge is not recorded, leading to difficulty of experience sharing and knowledge management. Therefore, this study intends on standardizing the prediction of parameters procedure and derives useful decision rules from multiple attributes.

Data preparation process will include data collection, data inspection and cleaning, data transformation and partition to ensure the data is in good quality and can be effectively analysed (Lee & Chien, 2022). First, three types of data will be collected based on domain knowledge, including abnormality data, product data and troubleshooting solution data from historical probe card fault cases.

- Abnormality data: The abnormality data will include the abnormal situation of the probe card and on-site testing fail items of the fault cases.
- Product data: The product data is the basic information related to each probe card, including product type, design house for the tested wafer, customer and tester type.
- Solution data: The troubleshooting solutions for the fault cases are regarded as the solution data. The solution data will contain the solution codes and its effectiveness of solving the abnormal situation.

Second, consistency and completeness of the data is checked by correcting errors, removing noise and deleting incomplete objects. Third, the data will be transformed into analytical form with condition and outcome attributes. Fourth, the collected data will be partitioned into training dataset (k%) and testing dataset (100-k%), where the decision rules will be derived from the training dataset and the testing dataset.

2.5.4 Conclusion

Focusing on realistic needs, so far, it can be concluded that an AI based framework that integrates RST and domain knowledge to systematically derive decision rules from incomplete information including the abnormal situations and product information to suggest prioritized solutions for probe card troubleshooting is the need of the hour. Indeed, probe card that serves as the testing signal interface between the tester and wafer is an indispensable component to ensure the integrity of IC testing that is increasing challenging owing to the shrinking IC feature sizes. The possible main contribution and novelty of this research can be summarized as follows: Firstly, domain knowledge and troubleshooting know-how will be effectively incorporated for defining the condition attributes for developing an AI model and validating the derived rules. Secondly, an empirical study will conducted for validation in a leading probe card manufacturer, in which the results have shown practical viability of the proposed approach. Indeed, the reducts and the rules derived by this AI model can provide effective suggestions for the engineers to shorten the troubleshooting time and reduce the equipment downtime. Thirdly, this validated solution will be embedded in the digital decision system that is implemented in real settings. The probe card manufacturers can effectively employ this proposed solution to integrate domain knowledge and troubleshooting experience that can reduce the loss of core know-how.

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2.6 DC13: AI-assisted study and forecast of field performances of probe cards for EWS applications

Semiconductor manufacturing has become increasingly complex with the continual minimization of critical dimensions in accordance with Moore's Law. This has led to escalating intricacy and expenses associated with testing and packaging integrated circuits (ICs) [1]. Within the manufacturing process, probe cards fulfill an indispensable role in wafer probing by serving as the interface between the wafer under test and the automated test equipment (ATE). However, advances in semiconductor technology have amplified the complexity of probe card design, production, and troubleshooting. For instance, state-of-the-art probe cards may contain over 50,000 probe pins with pin pitches under 40 µm [2]. An example of a cantilever probe card is shown in Figure 17. Unexpected probe card failures during wafer probing can significantly reduce overall equipment efficiency and customer satisfaction. Therefore, developing effective solutions to evaluate probe card performance is critical for manufacturers. This research aims to establish an assessment framework leveraging predictive data-driven modelling, and experimental validation to enable robust analysis of probe card field performance.

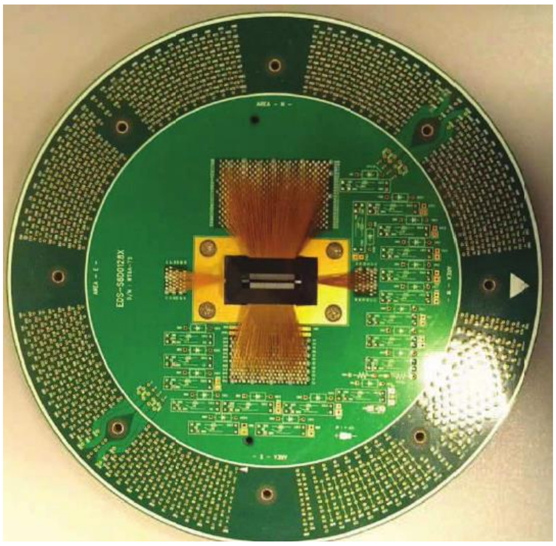


Figure 17: A probe card with cantilever pins [2].

Probe cards are a critical component used in testing semiconductor wafers (see Figure 18). They provide the electrical interface between the wafer under test and the automated test equipment. Probe cards contain an array of microscopic probe needles or "pins" that make physical and electrical contact with bonding pads on the dies on the wafer surface. State-of-the-art probe cards can contain over 50,000 probe pins with pin pitches under 40 µm. Different types of probe cards include vertical, cantilever, and MEMS designs (Figure 19).

During wafer testing, the probe card is positioned over the wafer under test. The wafer is then raised to contact the probe pins, allowing the ATE to perform tests by sending and receiving signals through the probe card pins. Probe cards must be precisely engineered to match the layout of each device under test.

By providing temporary electrical connections to the dies on the wafer, probe cards enable testing and verification of fabricated ICs before they are cut from the wafer and packaged. This helps identify defective dies early and avoid unnecessary packaging costs. The probe card is a consumable component that wears out over time and must be periodically inspected or replaced. Ensuring the reliability and performance of probe cards is therefore critical for semiconductor manufacturers.

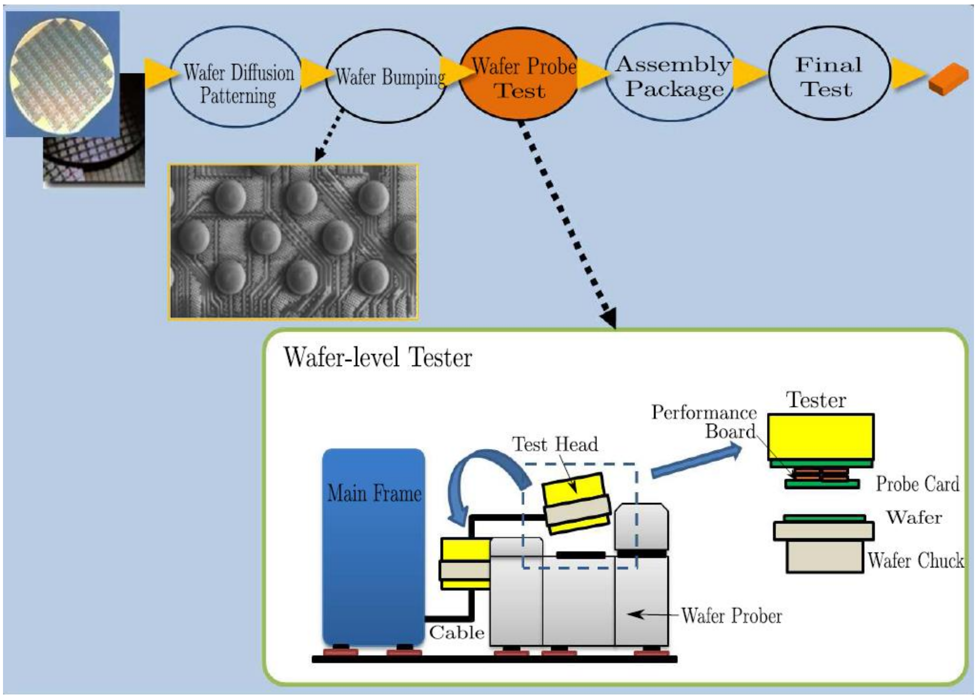
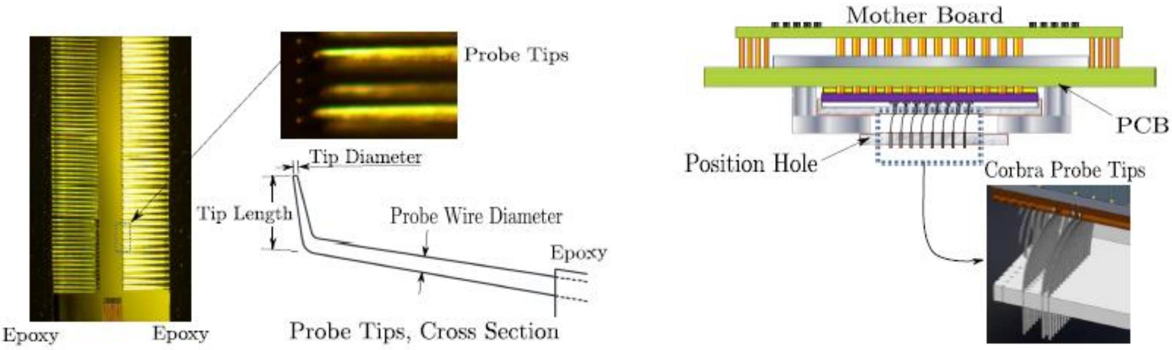


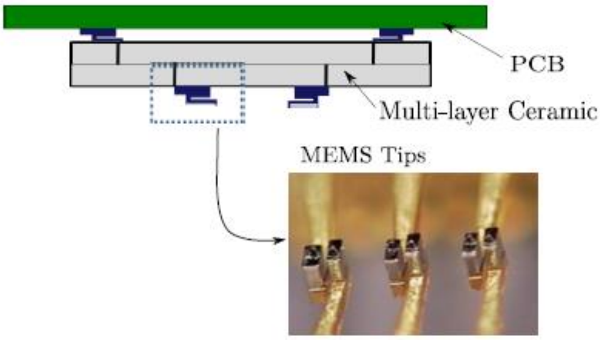
Figure 18: Schematic of the wafer-level test [2].

In summary, probe cards allow pre-packaging testing of IC wafers through precision electrical contacts with the dies. As a consumable component, probe cards require robust solutions to monitor and evaluate their ongoing field performance.



a) cantilever

b) vertical



c) MEMS

Figure 19: Cantilever, Vertical and MEMS type of probe card. (SDA Technology Co., Ltd.)

This literature review examines prior academic research related to:

1- Probe card technology and the associated challenges in wafer probing
2- Approaches for IC testing and fault diagnosis
3- Assessment of probe card field performance

By synthesizing key studies in these areas, current knowledge gaps are identified and opportunities for further research are discussed.

2.6.1 Probe Card Technology and Wafer Probing Challenges

As outlined by [3], probe cards have become integral components within semiconductor test processes due to the persisting influence of Moore's Law and the corresponding minimization of IC dimensions. Consequently, wafer probing and testing have grown more intricate. They underscored several trends amplifying wafer probing complications, including escalating memory density, shrinking chip sizes, rising number of die per wafer, and decreasing pad pitch. These factors have also led to a rapid increase in the number of probe card pins and stringent requirements for contact precision.

Adding to this, [4] delineated that semiconductor IC testing encompasses wafer probe testing utilizing a probe card as well as final testing of the packaged IC. The probe card serves to identify electrical specification deviations among the ICs under test. [5] delved deeper into measurement challenges associated with highly integrated products and miniaturization trends. They highlighted issues with probe card cleanliness, flatness control, and probe pressure. Integrating Six Sigma and TRIZ methodologies was recommended to address these obstacles.

Furthermore, [1] cautioned that shrinking IC dimensions have amplified the complexity of manufacturing processes and testing. For probe cards in particular, fault diagnosis during wafer testing can be time-intensive, extending up to 30 days in some cases. This prolongs machine downtime and negatively impacts productivity. Accordingly, there is a need for more effective and efficient approaches to probe card troubleshooting and performance evaluation.

2.6.2 IC Testing and Fault Diagnosis

To enhance the accuracy and efficiency of IC testing, researchers have explored various AI and statistical techniques for diagnosing faults in semiconductor fabrication equipment:

[6] proposed combining modular neural networks with Dempster-Shafer theory to improve fault detection and classification capabilities. [7] developed an expert system grounded in Bayesian networks to advance semiconductor equipment fault diagnosis. Their approach also incorporated novel methods for refining probability assessments.

[8] applied Bayesian networks along with principal component analysis to diagnose faults in etching tools. [9] utilized support vector machines to detect abnormalities, extract fault signatures, and categorize issues. [1] recently revisited Bayesian networks to model connections between diagnostic variables, specifically for diagnosing probe card faults.

A recent study by [10] proposed using autoencoders and event log data to detect abnormal behaviour in automatic test equipment. They developed a practical methodology and demonstrated its effectiveness on real-world semiconductor data. The autoencoder approach provides a novel way to leverage event log data to identify anomalies in ATE operation. This could enhance early fault detection and reduce wafer test times.

While these studies demonstrate the potential of AI, statistical modelling, and data mining to enhance semiconductor fault diagnosis, there remain substantial gaps in research when it comes to data-driven assessment of probe card performance in the field.

2.6.3 Assessment of Probe Card Field Performance

Very few studies have concentrated specifically on evaluating probe card performance under real-world operating conditions:

[2] developed a micro-vision system using 20X magnification optics to inspect cantilever probe pins with approximately 5-10 μm tip diameters. Their approach aimed to improve analysis speed using continuous stage motion rather than stop-and-go imaging. However, motion blur and latency issues were barriers to precision inspection during motion. Shin adopted basic image restoration and real-time triggering to partially address these challenges. While valuable, their work was limited to simple deblurring and did not provide a complete framework for high-speed analysis.

[11] developed a neural network forecasting model fed by production, maintenance, and repair data to predict probe card lifetimes and determine optimal replacement timing. Their model provided a data-driven approach for managing inventory and consumable parts.

[12] conducted proof-of-concept experiments showing the promise of using neural networks to analyse health data from fabrication equipment and forecast maintenance needs. Still, more research is required to validate these techniques on actual manufacturing systems.

[13] proposed a data-driven framework integrating rough set theory and domain knowledge to improve decision-making for probe card troubleshooting. Their approach enhanced diagnosis efficiency and reduced risks.

[14] proposed a machine learning approach to distinguish between test-induced and fabrication-induced defects by analysing spatial patterns in wafer test data. Their method achieved over 97% accuracy on real wafer products.

Cheng et al. and Chien and Wu demonstrate valuable data-driven techniques for identifying probe card issues using wafer test data characteristics. Integrating these approaches with predictive modelling of probe card field performance could further bolster troubleshooting and quality control capabilities. However, comprehensive research combining multi-factor modelling, experimental validation, and leveraging operational data remains limited in current literature.

In summary, while progress has been made, there are still opportunities for impactful research contributions through developing an integrated AI/ML-based framework for probe card field performance assessment, validated by real-world data. The papers by Cheng et al. and Chien and Wu provide useful foundations in this direction.

2.6.4 Conclusion

Based on this review, probe cards are indispensable components in semiconductor wafer testing, but continual advances in process technology have radically increased the complexity of probe card design, troubleshooting, and performance evaluation. Prior research provides meaningful foundations in IC fault diagnosis and the potential of AI/ML techniques. However, focused research on predictive modelling and experimental validation of probe card field performance is scarce. Developing a robust data-driven assessment tool for probe card manufacturers would provide significant value to industry by improving product quality, reducing risks, and strengthening customer satisfaction. This highlights a prospective area for further research and contributions.

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3 Future work

In WP4 Physics of degradation, test methods will be developed to gain an understanding of the physics of relevant failure mechanisms and to identify material and process un-certainties. The specific aims are as follows:

- Identification of uncertainties of all analysed materials and processes applied within the research projects and summary of the findings in a common database.
- Description of the degradation development behaviour as input for the physics-informed learning (function or interrelation).

Additionally, measurement data will be generated as a basis for WP6.

In this deliverable, 6 DC’s have described the outcomes of their literature review:

- DC1: Criticality assessment methodology for PCBA features by Vikram Kamble

  The future work of this DC will focus on the degradation patters in PCB level microvias as microvia degradation and failure is not properly understood.

- DC4: Accurate digital twins on component level by Alireza Mehrabi

  The future work of this DC will focus on the development of a new real-time digital twin model with the ability to classify faults in the device based on the detection of abnormal performance.

- DC6: Reliability of IC packages under small loading conditions by Mohammad Musadiq

  The future work of this DC will focus on qualifying microelectronic product that require long lifetimes, e.g., 100khrs and beyond, under an application load that is repetitive but not high (or harsh, typically $\Delta T < 10$degC). How can one qualify for such circumstances and what test strategies are available and/or required?

- DC10: Microstructure Informed Modelling and AI for Reliability Predictions by Najeem Muhammad Umair

  The future work of this DC will focus on employing thermo-mechanical damage modelling at the microstructure level, for example using crystal plasticity model, for Sn-based Pb-free solders is underscored, considering aspects such as heat activation and back stresses.

- DC12: AI-assisted design of high-performance and high-reliability probe technologies for EWS applications by Imtiaz Shehryar

  The future work of this DC will focus on providing an AI based framework that integrates RST and domain knowledge to systematically derive decision rules from incomplete information including the abnormal situations and product information to suggest prioritized solutions for probe card troubleshooting.

- DC13: AI-assisted study and forecast of field performances of probe cards for EWS applications by Bejani Mehidi

  The future work of this DEC will focus on developing a robust data-driven assessment tool for probe card manufacturers to provide significant value to industry by improving product quality, reducing risks, and strengthening customer satisfaction.

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